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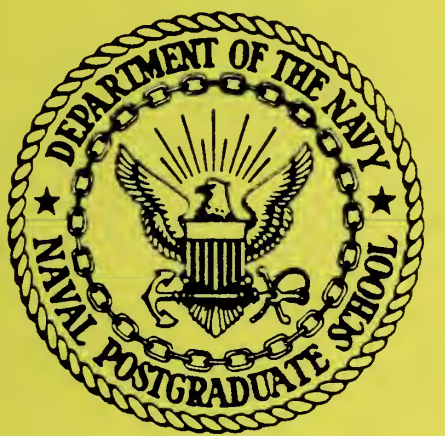

FREQUENCY RECEIVERS IN THE SATELLITE

COMMUNICATIONS SIGNAL ANALYZER

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PROJECT REPORT

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Design and operation is presented of the Frequency Receivers to be incorporated into the Satellite Communications Signal Analyzer (SSA) under development by the Naval Postgraduate School, with the sponsorship of the Naval Electronic Systems Command. The receivers have a linear dynamic range of 130 decibels, permit frequency measurement accuracy to ± 0.01 Hz, and process received RF for display in signal vector format.

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ABSTRACT

Design and operation is presented of the Frequency Receivers to be incorporated into the Satellite Communications Signal Analyzer (SSA) under development by the Naval Postgraduate School, with the sponsorship of the Naval Electronic Systems Command. The receivers have a linear dynamic range of 130 decibels, permit frequency measurement accuracy to $\pm$ 0.01 Hz, and process received RF for display in signal vector format.

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I. INTRODUCTION

The Frequency Receiver designed for the Satellite Communications Signal Analyzer (henceforth SSA) is an adaptation of the A6 receiver in the experimental version of the SSA /Ref. 1, 2/. Use and experimentation with the A6 receiver led to the functional and performance criteria upon which this receiver was designed. Although the concepts of the two receivers are similar, the implementation of them was not. The newer receiver offers far greater versatility in performance of the functions that were considered most useful to the SSA, determined by experimentation with the A6 receiver. These functions are presented, in general, in this section and in detail in succeeding sections.

A. REQUIREMENTS

1. Frequency Measurement

The primary purpose of the Frequency Receiver is to measure the carrier frequency of any received signal, either from a satellite or an interference source. This measurement is integrated into the other information processed by the SSA /Ref. 3/ to track transmitter performance of intended users, check satellite transponder and transmitter performance, and identify interfering signals. In addition, the frequency receiver is to be used to record each user's discrete carrier frequency (during that user's transmission burst) in a time divided multiple access channel such as the Information

Exchange Subsystem (IXS), or Demand Assigned Multiple Access (DAMA) system. Since transmitter frequency in DAMA is specified to be $\pm$ 100 Hz, with time bursts of 0.1 seconds it is desirable to measure frequency to $\pm$ 1 Hz accuracy within the 0.1 second burst in order to distinguish and track individual users. Correlation between the time of burst and the net controller will enable identification of frequency with user, so that any discrepancies discovered in the user's signal spectrum can be quickly and directly corrected.

2. X-Y Display

The second function of the receiver is to process the received signal for a display of it in vector format. This is done using an X-Y oscilloscope and mixing the signal down to baseband with a coherent mixing frequency. As such, a constant amplitude CW carrier appears as a dot at a distance from the oscilloscope center proportional to its amplitude. An amplitude modulated carrier appears as a dot at varying distance smeared to a radial line. PSK modulation appears as two lines, 180° apart; QPSK as four lines, 90° apart. Noise vectors appear as "balls" at the vector end, due to the random nature of noise and the storage time of the oscilloscope.

Since most satellite communications signals are phase shift modulated, such a display is useful in the SSA. It is also used as an aid in identifying interference signals.

B. IMPLEMENTATION

Both basic functions of the receiver were accomplished using a phase locked loop (PLL) design. References 4 and 5

cover design and operation of phase locked loops in depth. In this receiver an imperfect second order long loop was designed. The "long" implies the mixing of the signal to base band by a reference frequency (50 kHz) source in the loop, rather than a direct mixing to base band by the VCO. This allowed narrow bandwidth (200 Hz) IF filtering since the coherent nature of the loop would force the signal spectrum to always be centered in the pass band, and at 50 kHz permitted the use of lumped filters for the wider bandwidth (10 kHz, 3 kHz) filters as opposed to more expensive crystal filters at the 29 MHz or 1 MHz IF stage. A second order transfer function was chosen to minimize phase error, and its performance was demonstrated in the A6 receiver. The "imperfect" second order loop was chosen here to eliminate the VCXO control voltage drift in no-signal conditions due to voltage offsets, a problem in the A6 receiver. It is desirable to keep the VCXO at center frequency in the absence of signal to enable quicker lock up in time burst system reception (IXS, DAMA). Since the receiver is coherent, proper selection of hardware components would result in the necessary frequency measurement accuracy. The coherent processing is also exactly what was needed for the X-Y display, and a PLL facilitates reception of typically weak satellite signals.

A design to implement signal processing for quick (< 0.1 seconds) and accurate ($\pm$ 1 Hz) frequency measurement, and for the X-Y display is the topic of this thesis. Frequency measurement is best done in a PLL using non-linear signal

processing (limiter), since frequency not amplitude content is of prime consideration. An X-Y display is most useful if the signal amplitude content is preserved (linear signal processing). In this way signal fading can be observed, as well as amplitude modulation. Some form of gain control was also desired since the range of input signals possible can not be displayed meaningfully on a four inch diameter fixed range oscilloscope such as the X-Y display.

Both functions are accomplished by doing linear processing in an IF stage at 29 MHz and 1 MHz, filtering in a 50 kHz IF stage, then splitting the signal. One branch is routed through a limiter and carrier extraction circuit to be processed by the PLL (Fig. 1). The other branch is routed to a linear X-Y amplifier. Course gain control is provided at the 29 MHz IF stage in three discrete steps (5 dB, 40 dB, 70 dB), and scaling gain control in the X-Y display amplifier in 5 dB steps. The step attenuators in the 29 MHz IF stage, besides course gain adjustment, also provides absolute calibration of the X-Y display to 0.5 dB, by having digitally controlled $\pm$ 5 dB attenuator adjustment in 0.5 dB steps about the primary step. The gain control was designed to provide maximum use of the X-Y display, yet keep the signal level high enough to drive the limiter to enable maximum performance of the PLL.

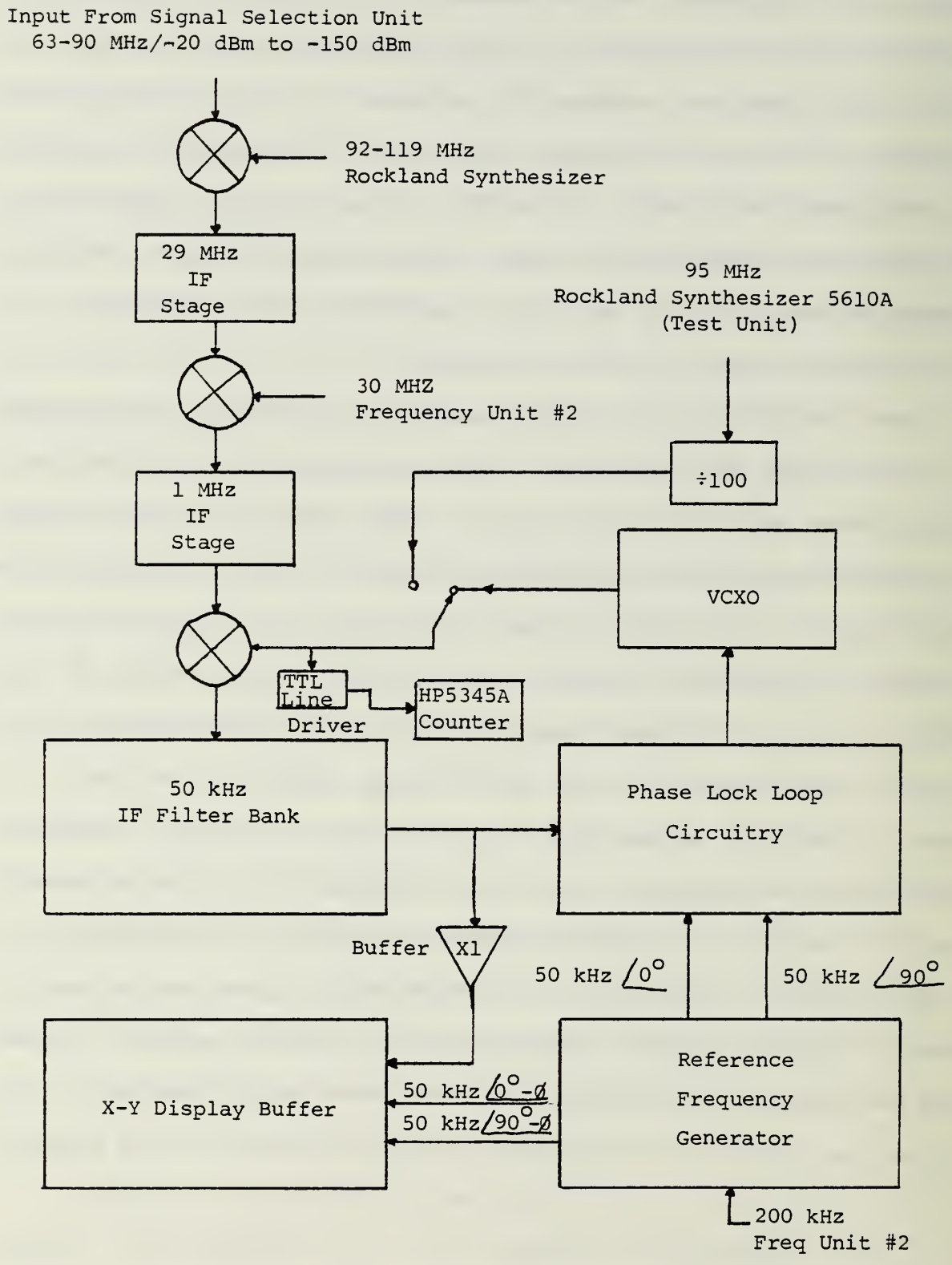


Figure 1

Frequency Receiver Block Diagram

II. IF AMPLIFIER

A. GENERAL

A detailed explanation of the IF stage in the Frequency Receivers follows. Design tradeoffs made in selection of components, gain and noise calculations are presented. Assuming low noise, wideband (>30 kHz) linear signal processing from the antenna to the signal selection unit where the receiver receives it's input, it is the IF stage that determines the dynamic range, and noise performance. It must provide sufficient gain to amplify the smallest signals of interest, but keep gain low enough to prevent saturation of components with the largest signal of interest. It must have a low noise figure. It determines the receiver bandwidth. It affects frequency selection and channel isolation. It must be cost-effective and meet a development schedule (Table I).

The design was further complicated by the unpredictable nature of the signal inputs, since the receiver will be used to identify RFI as well as the known satellite signals, and by the linear versus non-linear processing tradeoffs discussed in section I.

B. DESIGN TRADE-OFFS

Two designs for the IF stage were seriously considered. The first was rejected, and perhaps is of no further consideration, but sifficient time was spent in its development that it is worth mentioning here as background for the

Dynamic Range	:	130 dB
Lowest Input Signal Power	:	-150 dBm
Highest Input Signal Power	:	-20 dBm
IF Bandwidths	:	30 kHz, 10 kHz, 3 kHz, 200 Hz
PLL Bandwidths	:	1000 Hz, 300 Hz, 100 Hz, 20 Hz
Received Carrier Accuracy, IXS DAMA	:	$\pm$ 1000 Hz $\pm$ 100 Hz
Input Signal Modulation	:	AM, CW, Binary PSK, QPSK

TABLE I

FREQUENCY RECEIVER SPECIFICATIONS

reasoning in the selection of the final design.

1. AGC/MGC

A manually controlled AGC loop was first considered. Pure AGC is unsatisfactory for the X-Y display, since no comparative data between different signals can be obtained. A manual control was designed whereby the AGC control voltage was the sum of three control voltages; a MGC voltage, a high level AGC voltage, and a low level AGC voltage. The MGC voltage set a range about which the IF stage was a linear amplifier. If the signal got too strong the high level AGC voltage became a factor and reduced gain. If the signal dropped to a level that could no longer drive the PLL limiter into limiting, then the low level AGC voltage resulted in increased gain. Signal processing was linear between the high and low level AGC detector thresholds, with the signal visible on the X-Y display. Signals stronger or weaker than the high or low levels were either off scale on the display or too small to distinguish, respectively. The design was rejected for two primary reasons. One, frequency measurement accuracy depended upon the MGC setting. If it was properly set frequency measurement was accurate. If it was set too low (minimum gain reduction) then the high level AGC would effect gain reduction for large signals in order to prevent component saturation. If the input signal was amplitude modulated there was an indeterminable amount of amplitude to phase modulation conversion in the AGC components that resulted in a frequency measurement inaccuracy. Second, a slow AGC loop would alleviate the first problem, but would result in possible component

damage if the MGC control was set too low and a very strong signal burst in. If the AGC did not respond fast enough, at minimum the receiver would be driven well into saturation and effectively shut down.

Compromise of the two was unresolvable, and the design was rejected in favor of pure MGC in discrete steps.

2. Stepped MGC

This design eliminated the problems of the previous design. Three signal level ranges are implemented for processing (Fig. 2). All signals of a power level within the range selected are processed linearly for the X-Y display. Any signal level higher that the range maximum causes saturation, but this non-linear processing does not affect the PLL frequency measurement, and the presentation on the X-Y display is off scale, cueing the operator to shift ranges if an X-Y presentation is desired. Signal levels smaller than the range minimum are not detected by the PLL until the operator changes ranges. There is no warning of this condition other than the receiver unlock indication and no X-Y display presentation. The width of each range (65 dB) was determined by the dynamic range of the limiter in the PLL (sec. III. C.). Range selection is made in the 29 MHz IF stage for two reasons. First, high gain is required for small signal levels, but this gain would result in saturation of downstream components with large signals unless the gain is reduced (or attenuation increased). The attenuators both select the signal-level band and prevent saturation. Second, the solid state attenuators available operate at this higher frequency range (29 MHz).

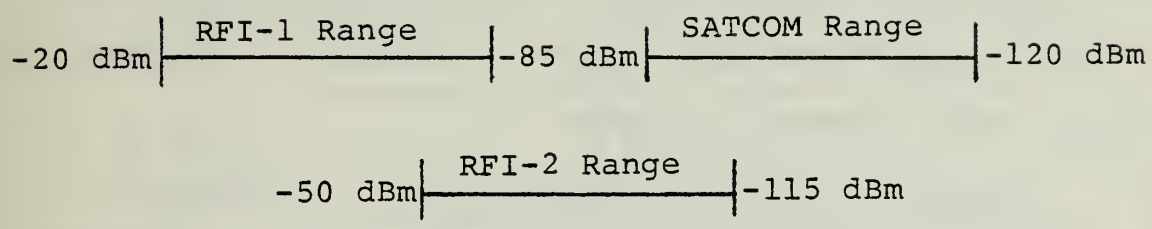


Figure 2

Frequency Receiver Input Power Ranges

C. 29 MHz IF STAGE

Figure 3 describes the 29 MHz IF stage. Calculations verifying the gain and noise performance of this configuration follow. During actual design, several iterations between gain/noise performance and component selection were made, but only the final figures are shown.

1. Saturation Levels Calculations

When considering component saturation levels four situations were considered (Table II):

a. Maximum signal input (-20 dBm) with GC 1 and GC 2 set at their minimum values (insertion loss only). Here power levels were checked to be below component destruction levels.

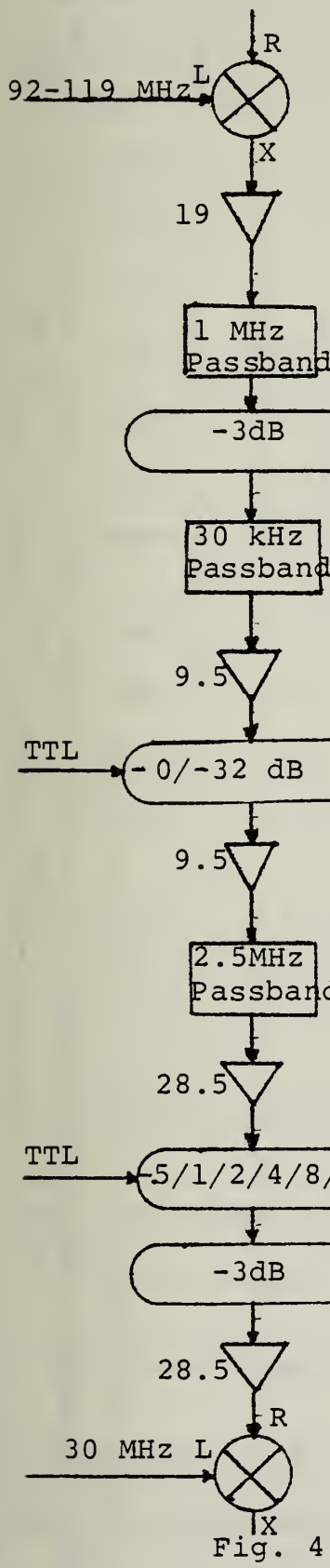
b. Maximum signal input (-20 dBm) with the receiver configured for the RFI-1 range. Here power levels were checked below component saturation levels (output power <1 dB compression point output power), ensuring linear signal processing.

c. Maximum allowable signal input with the receiver configured for the RFI-2 range (-50 dBm). Operating levels were checked below saturation levels as in b.

d. Maximum allowable signal input with the receiver configured for the SATCOM range (-85 dBm). Operating levels were checked below saturation levels as in b.

2. Noise Temperature Calculations

Noise calculations were made in terms of the equivalent noise temperature (T_e) of each section as illustrated in Table III. The use of the variable attenuators results in different noise temperatures of sections 3, 4, and 5 of the table



COMPONENT #	DESCRIPTION
FR-IF29-M1	Merrimac DMM-4-250 Mixer (1 dB Gmp.=8dBm//I.L.=8dB)
FR-IF29-A1	Anzac AM-105 Amplifier (N.F.=5.5dB)(1dB comp.= 17dBm//Max RF in = 20 dBm)
FR-IF29-P1	K & L Tubular Filter 4B340-29/1.-0 (I.L. = 5dB)
FR-IF29-P1	ELCOM Attenuator/AT-50-3
FR-IF29-F2	TYCO Crystal Filter (I.L. = 8 dB) Model # 001-34-760
FR-IF29-A2	Anzac AM-102 Amp. (N.F.= 5.5dB)(1dB comp.=17dBm// Max RF in =22 dBm)
FR-IF29-GC1	Daico Step Attenuator 100C 1428-1D(I.L.-0.3 dB)
FR-IF29-A3	Anzac AM-102 Amplifier
FR-IF29-F3	K&L Filter: 4B50-29/2.5-0 (I.L. = 2.9 dB)
FR-IF29-A4	Anzac AM-108 Amp(N.F.= 5.5dB)(1dB comp=17.5dBm/ Max RF in=19 dBm)
FR-IF29-GC2	Daico Step Attenuator I.L.=2.4dB) 100D0589-6-A- .5,1,2,4,8,32
FR-IF29-P2	ELCOM Attenuator/AT-50-3
FR-IF29-A5	Anzac AM-108 Amplifier
FR-IF29-M2	Merrmac DMM-4-250 Mixer

Fig. 4

Figure 3

29 MHz IF Stage

COMPONENT	COMPONENT GAIN	II.C.1.a.	II.C.1.b.	II.C.1.c.	II.C.1d.
ANTENNA TO SSU	+26.5 dB	-20 dBm	-20 dBm	-53 dBm	-85 dBm
FR-IF29-M1	-8.0	6.5	6.5	-26.5	-58.5
A1	+19.0	-1.5	-1.5	-34.5	-66.5
F1	-5.0	17.5[1]	17.5[2]	-15.5	-47.5
P1	-3.0	12.5	12.5	-20.5	-52.5
F2	-8.0	9.5	9.5	-23.5	-55.5
A2	+9.5	1.5	1.5	-31.5	-63.5
GC1[9]	-0.3/-32.3/ -0.3/-0.3	11.0	11.0	-22.0	-54.0
A3	+9.5	10.7	-21.3	-22.3	-54.3
F3	-2.9	20.0[3]	-11.8	-12.8	-44.8
A4	+28.5	17.1[4]	-14.7	-15.7	-47.7
GC2[10]	-2.4/-35.4/ -34.4/-2.4	21.0[5]	13.8	12.8	-19.2
P2	-3.0	18.6	-21.6	-21.6	-21.6
A5	+28.5	15.6[6]	-24.6	-24.6	-24.6
M2	-8.0	21.0[7]	3.9	3.9	3.9
		10.0[8]	-4.1	-4.1	-4.1

1 Output is 0.5 dBm over 1 dB compression point.
2 Output is 0.5 dBm over 1 dB compression point - design compromise - some loss of linearity in upper end of RFI-1 Range.
3 Linear output would be 20.2 dBm, 3.2 dB above 1 dB compression point, estimate 20 dBm output.
4 2.9 dBm below obsolute maximum input of A4.
5 Linear output would be 45.6 dBm, 28.1 dB above 1 dB compression point, estimate 21 dBm output.
6 3.4 dBm below absolute maximum input of A5.
7 Linear output would be 44.1 dBm, 26.6 dB above compression point, estimate 21 dBm output.
8 Linear output would be 13 dBm, 5.0 dB above 1 dB compression point, estimate 10 dBm output.
9 Attenuation=Attenuator step + Device Insertion Loss.
10 Attenuation=Nominal Setting-Calibration Range+Insertion Loss(worst case).

TABLE II
GAIN/SATURATION LEVELS - 29 MHz IF STAGE

COMPONENT	dB COMPONENT NOISE FIGURE			(F) dB SECTION NOISE FIGURE			dB COMPONENT GAIN			(G) dB GAIN PRIOR TO SECTION			(Te) K NOISE TEMPERATURE		
Signal Selection Unit							26.5						500		
Section 1															
FR-IF29-M1 A1	8 5.5			13.5			-8 +19			26.5			13.9		
Section 2															
FR-IF29-F1 P1 F2 A2	5 3 8 5.5			21.5			-5 -3 -8 +9.5			37.5			7.2		
Section 3	SATCOM	RFI-2	RFI1	SATCOM	RFI-2	RFI-1	SATCOM	RFI-2	RFI-1	SATCOM	RFI-2	RFI-1	SATCOM	RFI-2	RFI-1
FR-IF29-GC1 A3	0.3 5.5	0.3 5.5	0.3 5.5	5.8	5.8	5.8	-0.3 9.5	-0.3 9.5	-0.3 9.5	31	31	31	0.6	0.6	1388
Section 4															
FR-IF29-F3 A4	2.9 5.5	2.9 5.5	2.9 5.5	8.4	8.4	8.4	-2.9 28.5	-2.9 28.5	-2.9 28.5	40.2	40.2	8.2	0.2	0.2	260
Section 5															
FR-IF29-GC2 P2 A5	12.4 3 5.5	47.4 3 5.5	45.4 3 5.5	20.9	55.9	53.9	-12.4 -3 28.5	-47.4 -3 28.5	-45.4 -3 28.5	65.8	65.8	33.8	0	29.7	29675

TABLE III
NOISE TEMPERATURE - 29 MHz IF STAGE

depending upon which range the receiver was configured for (RFI-1, RFI-2, SATCOM). Worst case was considered, meaning the attenuators were set for maximum calibration attenuation (range value +5 dB), [see I.B.]. Equivalent noise temperature (T_e) was computed from the relation [Ref. 6]:

$$T_e = 290 \frac{(F-1)}{G}$$

where F is the noise figure of the section, and G is the power gain prior to the section. A convenient comparison point is a -85 dBm input signal, which is common to all ranges. From

$$SNR = \frac{C}{kTB}$$

where SNR is the signal to noise ratio at the output of the 29 MHz stage (A5), and

C = -85 dBm

k = -199 dBm/K-Hz

B = 45 dB Hz (30 kHz - widest IF filter)

$T = \sum_{i=0}^{5} (T_e)_i$; i = section number [Table III]

it is found that in the

SATCOM Range, SNR = 41.8 dB

RFI-2 Range, SNR = 41.6 dB

RFI-1 Range, SNR = 23.9 dB

As far as the frequency tracking loop is concerned, these levels of SNR are very adequate. Observing a -85 dBm signal on the X-Y display in either the RFI-2 or SATCOM range presents essentially the same picture. Viewing it with the

RFI-1 range selected presents it as a noisier signal. For this reason the SSA Operator will not be able to select -60 dBm to -80 dBm as X-Y display maximum deflection, when operating in the RFI-1 range /see Section VI/.

3. Gain in the Normal Operating Mode

The gain of the 20 MHz stage was determined so that any additional gain required to get the signal up to the minimum input for limiting, could be added in following IF stages (1 MHz, 50 kHz). In the calculation three considerations were noted:

a. the component gain values used in Table IV, are manufacturer's worst case specifications in mose cases.

b. the attenuators (GC1 and GC2) were set at the nominal calibration value.

c. the resultant gain was calculated for the SATCOM range only, and will be applied to the SATCOM range maximum (-85 dBm) and minimum (-150 dBm) signal inputs to compute the voltage levels (see paragraph D). It is easily shown (Table II) that the voltage levels so calculated will be the same for the maximum and minimum of the RFI-1 and 2 range, since signal level change between ranges equals attenuator change.

D. 1 MHz IF STAGE

The design effort and complexity of the 20 MHz IF stage ultimately resulted in a relatively uncomplicated 1 MHz IF stage (Figure 4). Similar calculations as in the 29 MHz stage, of saturation levels, noise temperature, and normal operation were made. The gain of the LM318 (A6) was the only degree of

COMPONENT		GAIN(dB)
Signal Selection Unit		+26.5
FR-IF29 -	M1	-8
	A1	19
	F1	-5
	P1	-3
	F2	-8
	A2	+9.5
	GC1	-0.3
	A3	+9.5
	F3	-2.9
	A4	+28.5
	GC2	-7.4
	P2	-3
	A5	+28.5
	M2	-8
TOTAL		+75.9 dB

TABLE IV

NORMAL GAIN - 29 MHz IF STAGE

Fig. 3

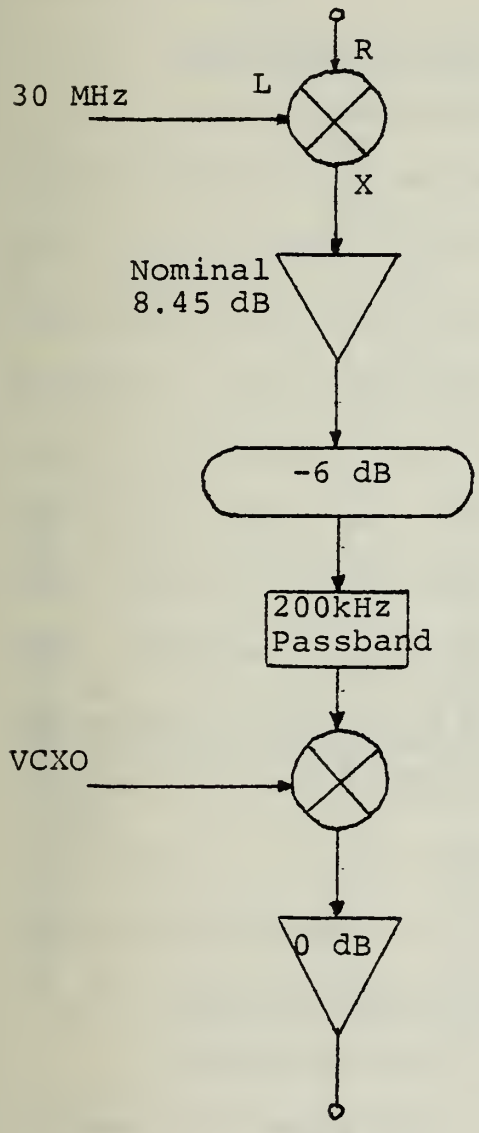
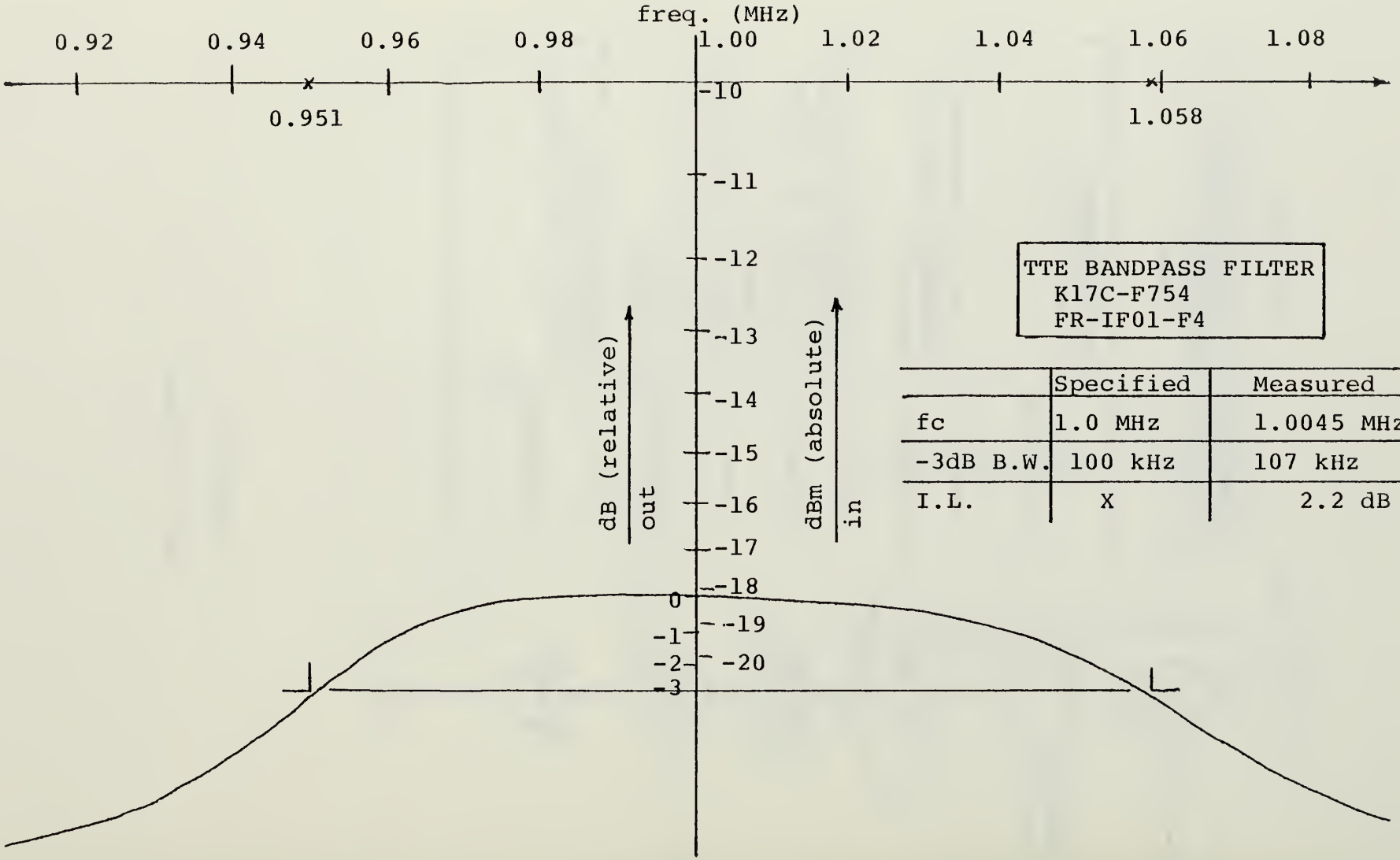


Fig. 8

COMPONENT	DESCRIPTION
FR-IF29-M2	Merrimal DMM-4-250 Mixer
FR-IF01-A6	LM 318 OPAMP GAIN=8.45 dB ± 5
FR-IF01-X1	Impedance Matching Network
FR-IF01-F4	TTE Bandpass Filter/ K17C(Fig. 5) (I.L.= 2.2 dB//1 dB amp = 13 dBm)
FR-IF01-M3	MC1496 - GAIN=22 dB (1 dB comp.=120 mV input)
FR-IF50-B1	TL083CN OPAMP (Unity Gain Buffer)

Figure 4

1 MHz IF Stage



	Specified	Measured
fc	1.0 MHz	1.0045 MHz
-3dB B.W.	100 kHz	107 kHz
I.L.	X	2.2 dB

Figure 5

FR-IF01-F4 Response Curve

freedom in this stage's design and was determined based on the 29 MHz normal gain (Table IV), and the gain of components up to the limiter.

1. Saturation Levels

Since voltage devices rather than power devices, as in the 29 MHz stage, are used it is convenient to convert the power level output of M2 to a voltage level. Table V is a continuation of the conditions described in paragraph II.C.1.a. through d., and tabulated in Table II, except that voltage levels are used. Four situations were checked for: (1) The LM318(A6) output was below 7 Vrms (saturation) in normal operation since $\pm$ 12 Vdc power supplied were used. (2) F4 (K17C, TTE, bandpass filter) output was below 4.47 Vrms, its 1 dB compressed output (+ 13 dBm). (3) The maximum input to M3 (MC1496) was below 80m Vrms, its 0.3 dB compression point (Figure 6). (4) The output of M3 did not saturate B1, the operational amplifier buffer following it ($\leq$7 Vrms).

2. Noise Calculations

Conversion back to noise figures in decibels was made to keep the results in the same terms as Table III. Table VI considers only the section up to the LM318 (A6), since no noise specifications are given for the MC1496 (M3). From these relationships /Ref. 6/ the noise figure (F) of the LM318 was calculated in decibels:

$$F = 1 + \frac{T_e}{T_o} \tag{1}$$

$$\text{noise power} = N_e = \frac{\overline{e_n^2}}{4R_s} = kT_eB \tag{2}$$

COMPONENT	VOLTAGE GAIN(V/V)	(rms) II.D.1.a.	(rms) II.D.1.b.	(rms) II.D.1.c.	(rms) II.D.1.d.
FR-IF29-M2	0.398	700mV	138.1mV	S	S
-IF01-A6	4.7/2.65/2.65/2.65	3.29V	365.0mV	A	A
-X1	0.5	1.65V	183.0mV	M	M
-F4	0.776	1.28V	140.0V	E	E
-M3	12.2[1]	2V[2]	1.73V		
-B1	1.0				

[1] Average value obtained from Figure 5 of gain below 80mV rms input

[2] Estimated output asimatoting curve in Figure 5

TABLE V

GAIN/SATURATION LEVELS-1 MHz IF STAGE

COMPONENT	COMPONENT NOISE FIG. dB			SECTION NOISE FIG. (F) dB			COMPONENT GAIN dB		
29 MHz IF+SSU							13.1	-21.9	-19.9
	SATCOM	RFI-2	RFI-1	SATCOM	RFI-2	RFI-1	SATCOM	RFI-2	RFI-1
FR-IF29-M2	8	8	8				-8	-8	-8
				16.6	16.6	16.6			
-IF29-A6	8.6	8.6	8.6				3.46	3.46	3.46

COMPONENT	GAIN ERROR TO SECTION (G) dB			NOISE TEMPERATURE (T_e) k		
29 MHz IF+SSU	65.8	65.8	33.8	521.9	536.8	31844
	SATCOM	RFI-2	RFI-1	SATCOM	RFI-2	RFI-1
FR-IF29-M2						
	78.9	43.9	13.9	0	0.53	528
-IF29-A6						

TABLE VI

NOISE TEMPERATURE - 1 MHz IF STAGE

$$\frac{\overline{e_n^2}}{B} = 4\, R_s k T_e \tag{3}$$

$$\sqrt{\frac{\overline{e_n^2}}{B}} = 10\text{nV}/\sqrt{\text{Hz}} \tag{4}$$

$$R_s = 1\text{k}\Omega \tag{5}$$

$$k = 1.38 \times 10^{-23} \text{ joules/K} \tag{6}$$

Equations (4) and (5) are obtained from the manufacturer's specifications [Ref. 7].

3. Normal Operating Mode Gain

As illustrated in Table VI, the nominal gain through the 1 MHz section is with A6 set to 8.45 dB. But its gain can be adjusted - 5 dB to compensate for actual gains and losses in the system up to the input of M3. For this reason the gain of the 1 MHz section is different for different receivers, but the total gain from the input of M1 to the input of M3 was nominally designed for, and is then adjusted to the value needed to have a voltage level of 80 mVrms when -85 dBm is input in the SATCOM Range, when -50 dBm is input in the RFI-2 Range, and when -20 dBm is input in the RFI-1 Range. Any further gain is applied through the 50 kHz filter bank to get up to the limiting levels of L1 (Figure 12).

III. 50 kHz ANALOG PROCESSING

A. ANALOG VOLTAGE MULTIPLIER

The MC1496 Balanced Demodulator is used as an Analoge Voltage Multiplier (AVM) in two places in the receiver. First, it is used as the mixer driven by the VCXO, down converting the signal at 1 MHz to 50 kHz. Second, it is used as the multiplier for the X and Y signal in the X-Y Display Driver. Operation of this device is explained in Refs. 8, 9, with the circuit employed an adaptation of the Product Detector shown. Gain performance of the modified circuit is plotted as Figure 6. The data obtained is consistent with the describing equations given in the references.

In its use as M3 in the frequency receiver the output is buffered through B1 because of the MC1496's inability to drive loads lower than 10 kΩ. Since only the difference frequency is of interest the output is AC coupled. The DC component was not meaningful at this point in the circuit.

In its use as M4 and M5 the DC component of the product is the information that is displayed on the X-Y oscilloscope (see VI. A.). The output is DC coupled through and filtered by F9 (or F10), which is DC biased to null the bias voltage at the MC1496 output (≈8.75 VDC). The oscilloscope X-amplifier and Y-amplifier adjustments are used to fine tune the nulling of the bias voltages. Configured as M4 and M5 the MC1496 is connected using 1μF capacitors in place of the 0.1μF

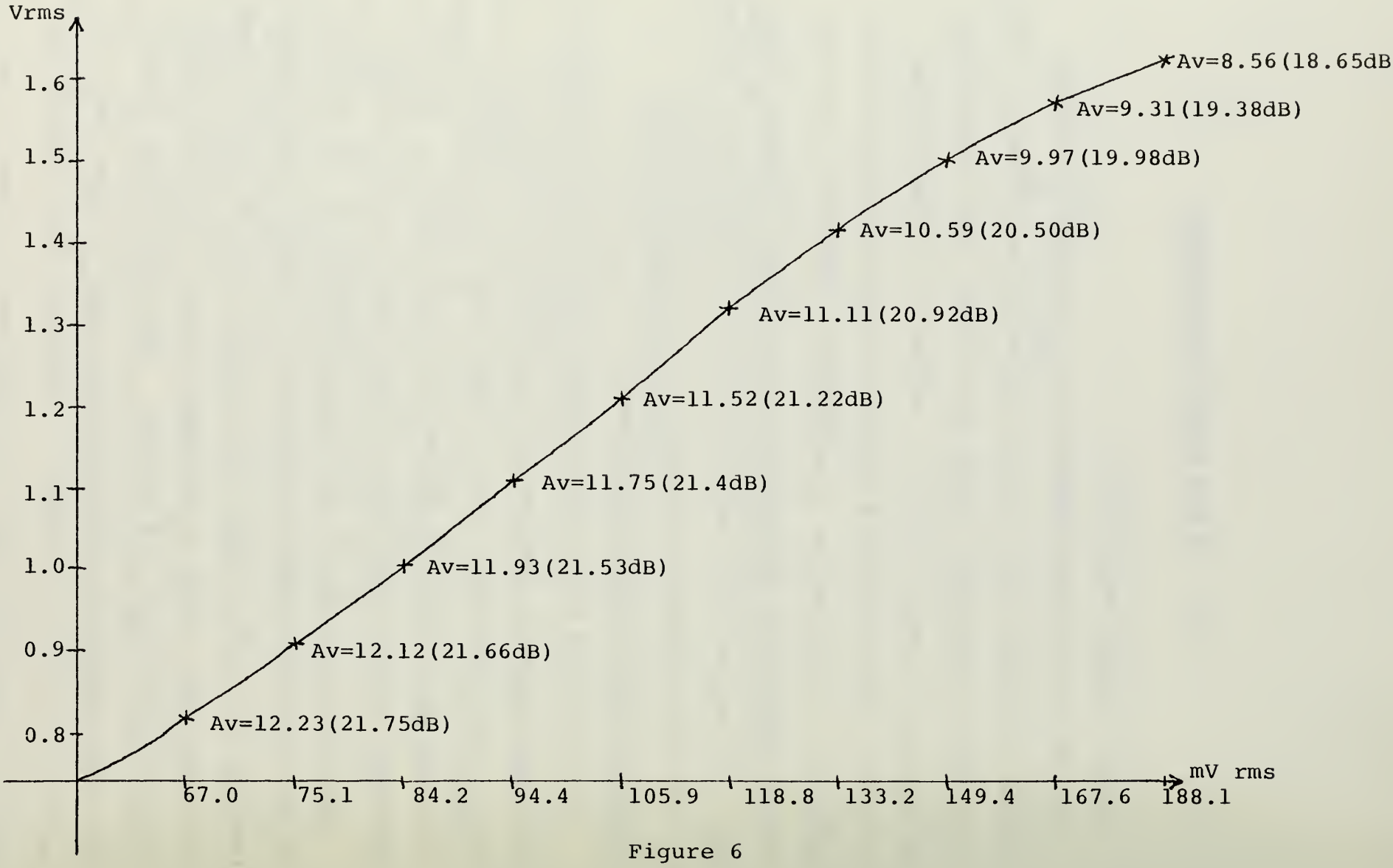


Figure 6

Input vs. Output Plot of MC1496

capacitors used in M3, as per Ref. 9, (Fig. 7).

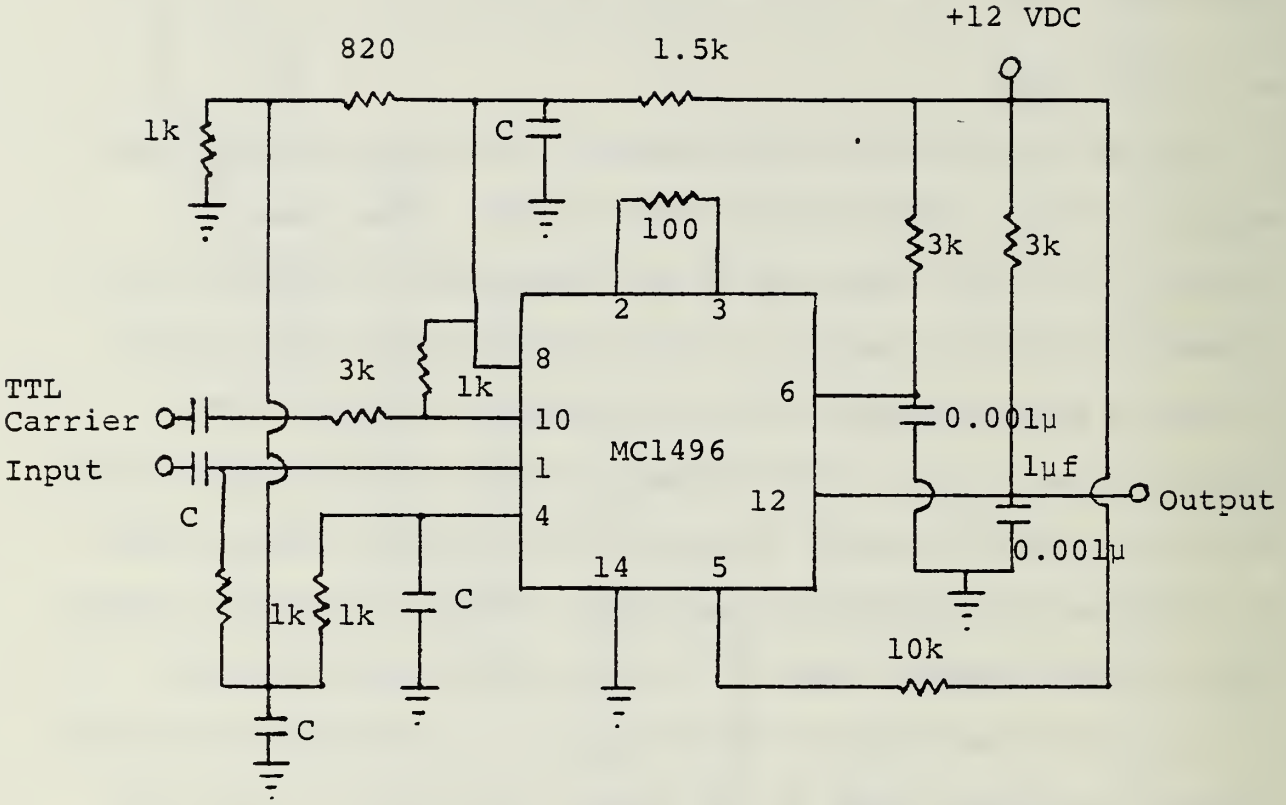
B. FILTER BANK

The 50 kHz IF filter bank enables selection of four bandwidths; 200 Hz, 3 kHz, 10 kHz, and 30 kHz. The response curves of the TTE 3 kHz and 10 kHz bandwidth filters are included as Figures 9 and 10. The 30 kHz filter (F2) is part of the 29 MHz IF stage, and is implemented using a DATEL active filter with a -3 dB lowpass cutoff of 85 kHz [Ref. 10]. An active filter is used following the straight through path to suppress any frequency components, other than signal, from reaching the limiter, such as carrier components from M3.

Since the receiver is calibrated it is important that gain through the filter bank be the same regardless of the filter selected. This explains the purpose of the amplifiers in the filter bank circuit (Fig. 8), since each filter has different conversion losses. The voltage gain of each circuit element is shown in Table VII. The straight through path is used as the reference. The voltage gain of the TTE filters is obtained from the response curves (Fig. 9, 10). The insertion loss of the 200 Hz filter is specified as 6 dB, but the voltage gain is not a simple conversion of 6 dB to a gain of 0.5 There is a mismatch between input and output impedances. If the filter has no insertion loss, then:

$$A_v = \frac{v_o}{v_i} = \sqrt{\frac{Z_o}{Z_{vr}}} = \sqrt{\frac{1 \times 10^3}{50}} = \sqrt{20}$$

Taking the conversion loss into account results in the value:



FR-IF01-M3	C=0.1 µF
FR-IFXY-M4	C=1.0 µF
FR-IFXY-M5	C=1.0 µF

Figure 7

Circuit Diagram For FR-IF01-M3 and FR-IFXY-M4/5

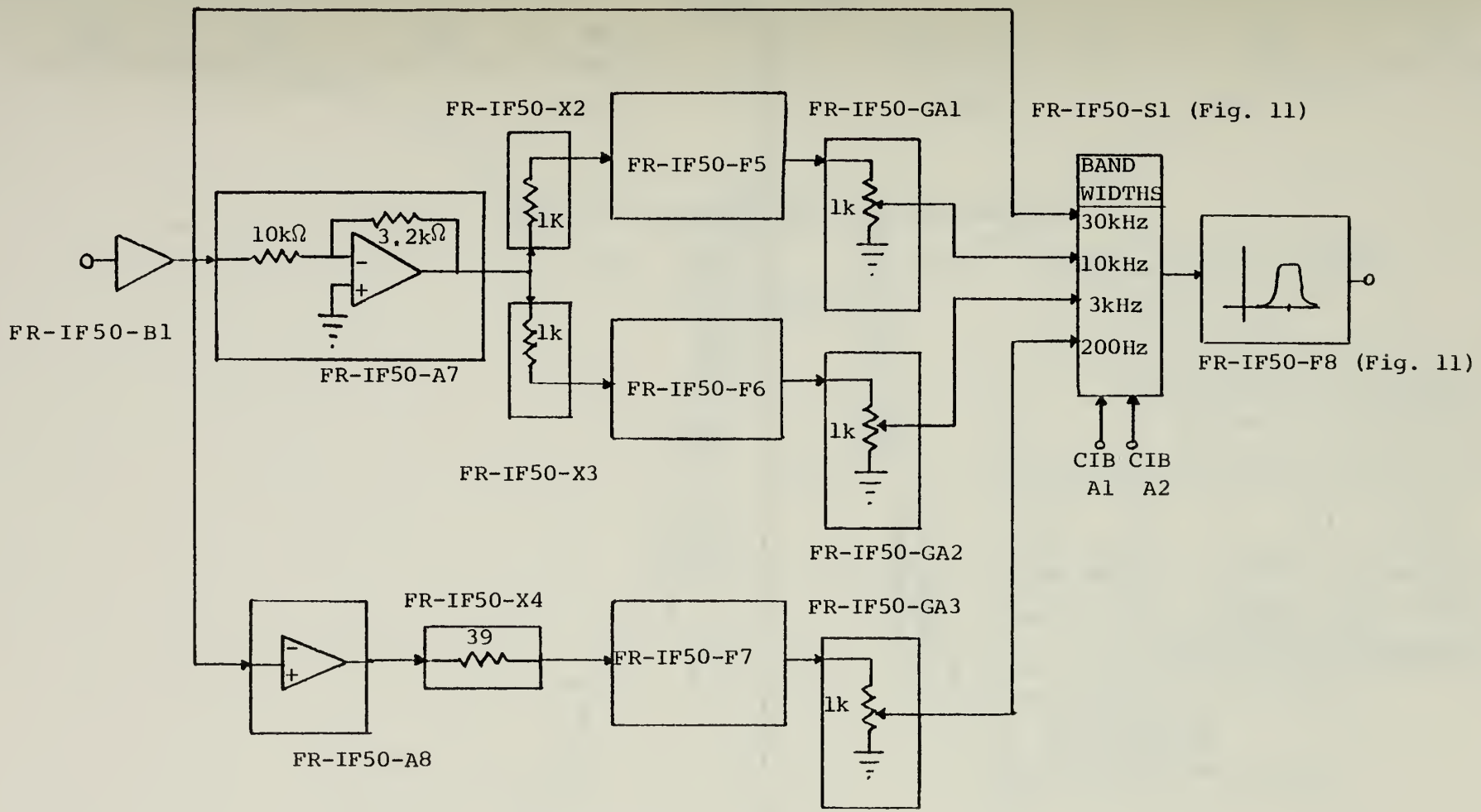


Figure 8

50 kHz IF Filter Bank Flow Diagram

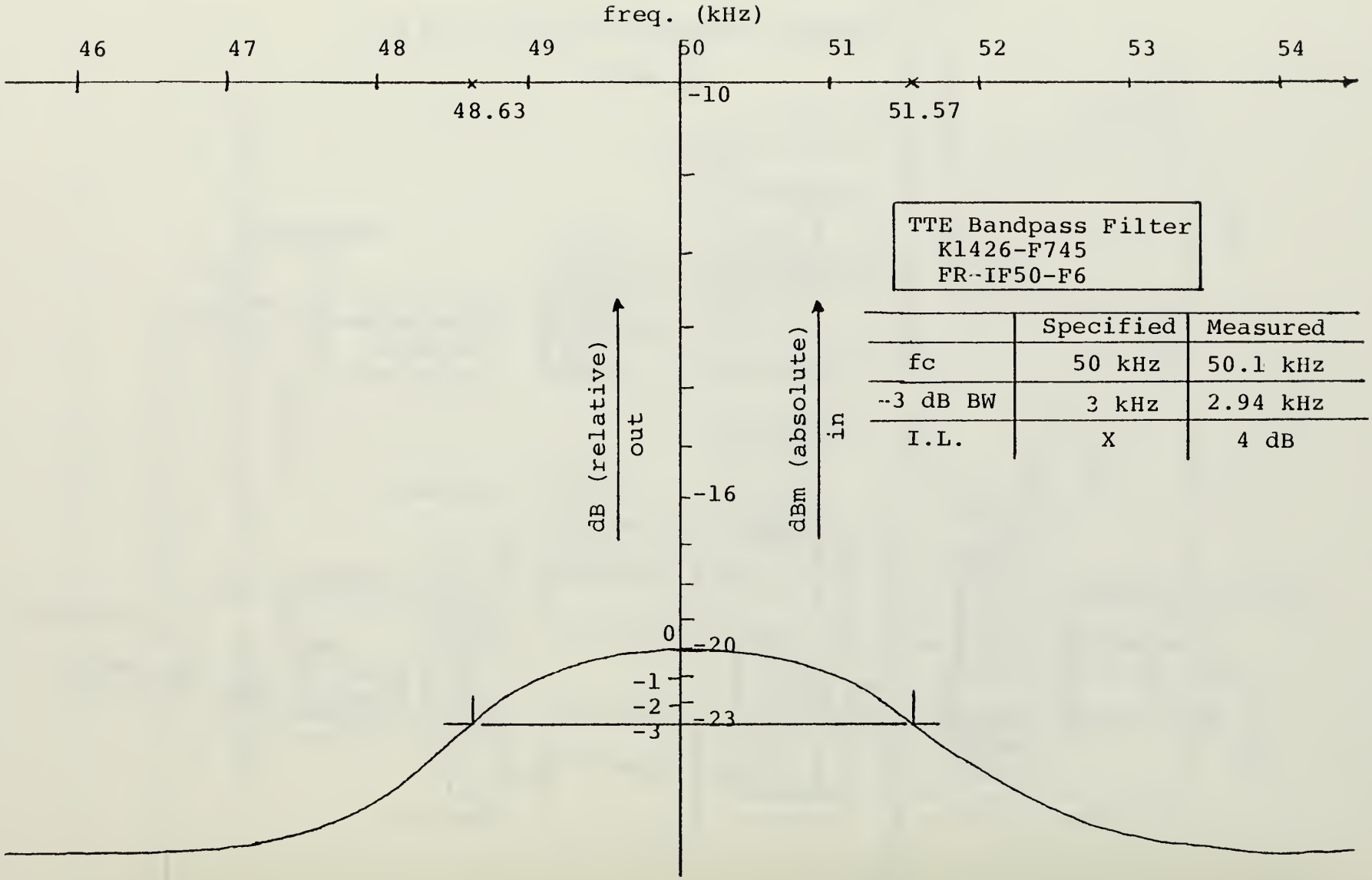


Figure 9

FR-IFSO-F6 Response Curve

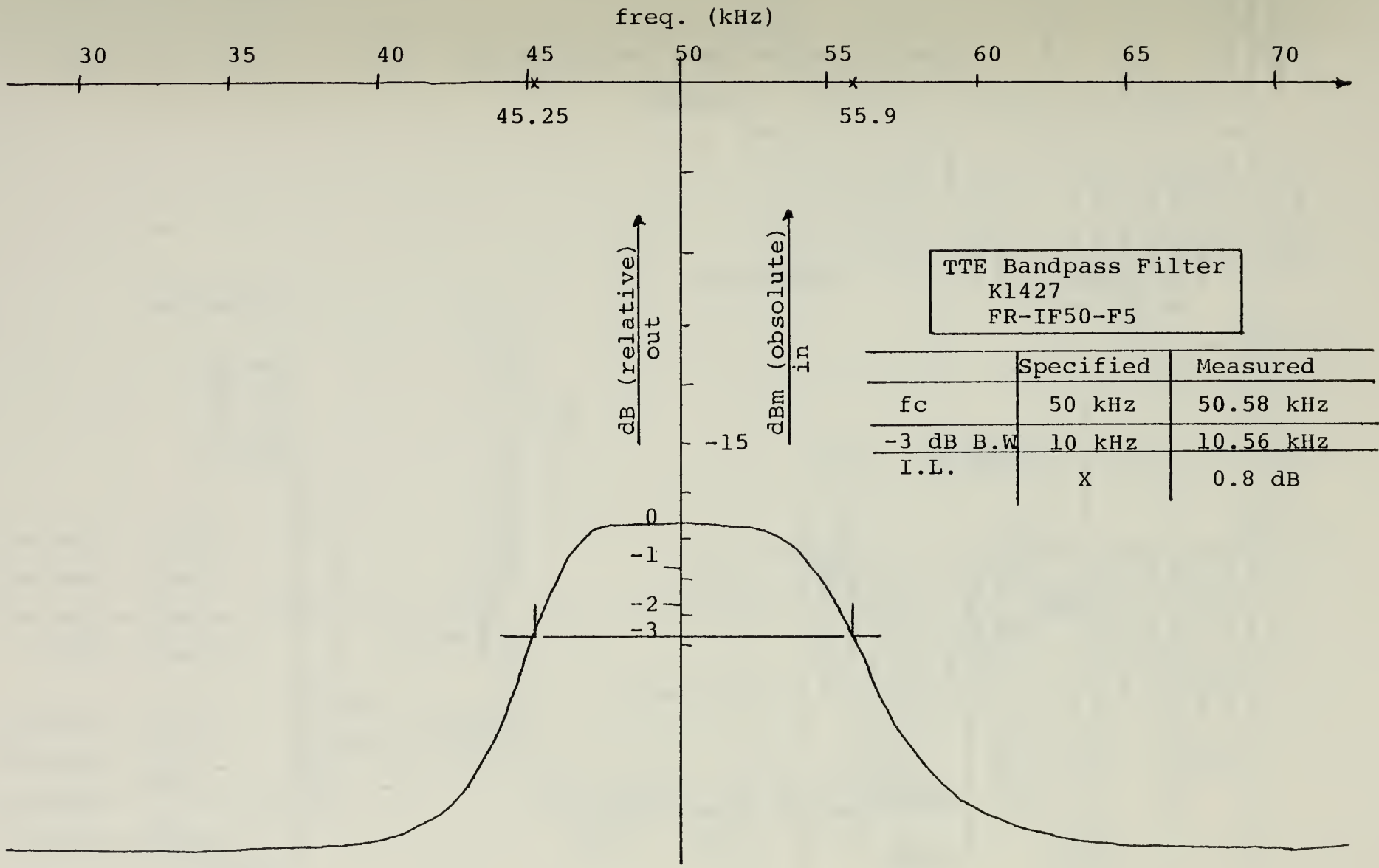


Figure 10

FR-IF50-F5 Response Curve

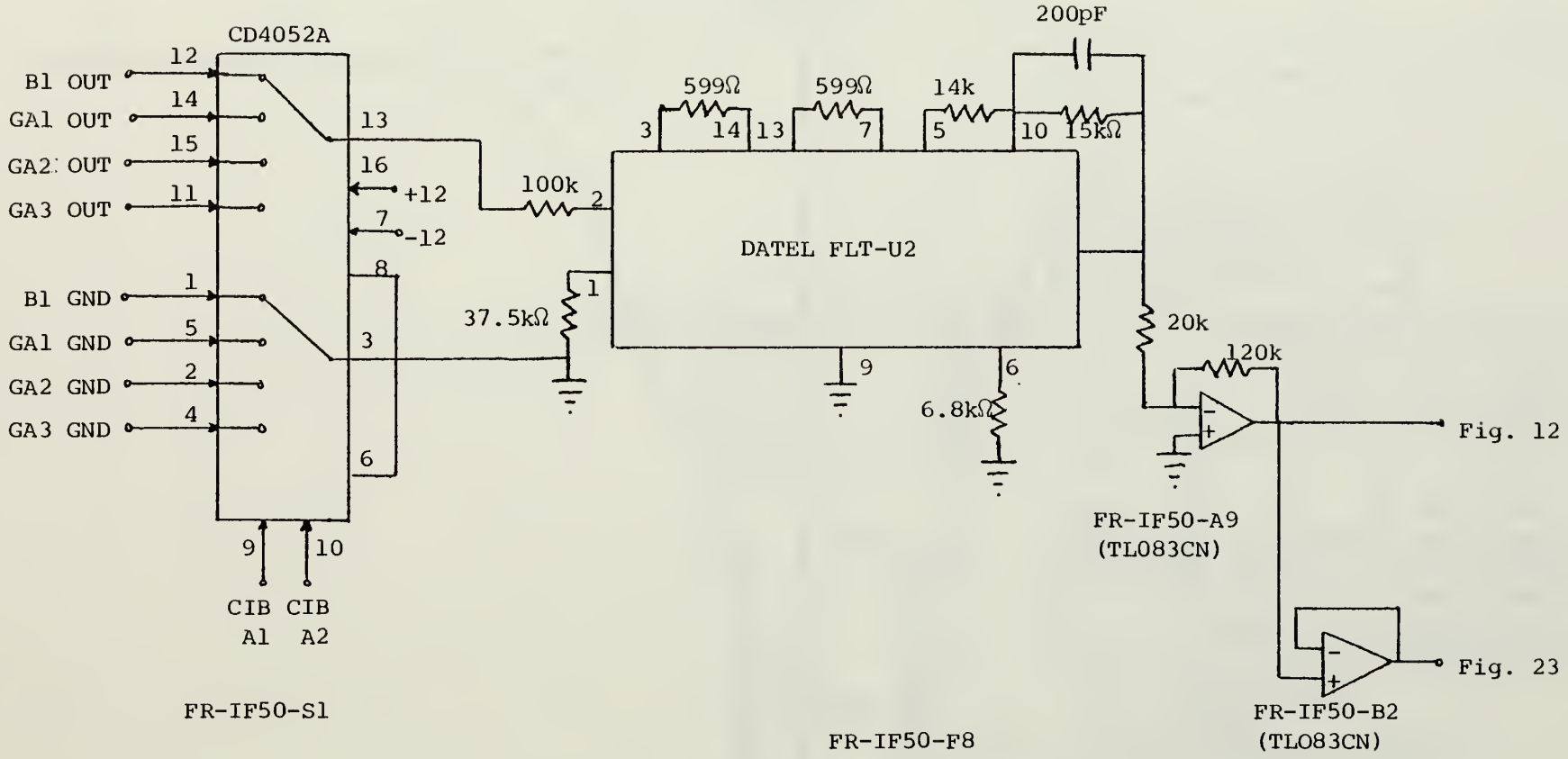


Figure 11

50 kHz Filter Bank Output Circuit

COMPONENT	(Max/Min) Input Level (rms)	Voltage Gain	Description
FR-IF50-B1	972mV/547mV	1	TC083CN OPAMP (TI)
A7	972mV/547mV	3.2	TC083CN OPAMP (TI)
X2	2.98V/1.68mV	0.5	1kΩ matching resistor
F5	1.49V/837uV	0.912	TTE K1427 BPF
GA1	1.34V/764uV	0.712	1kΩ trimpot
S1	972mV/547mV	1	CD4052AD-Analog Dip Switch(RCA)
F8	972mV/547uV	1.0	FLT-U2 Active Filter(DATEL)
A9	972mV/547uV	6.0	1kΩ matching resistor
X3	2.98V/1.68mV	0.5	1kΩ matching resistor
F6	1.49V/837uV	0.631	TTE-K1426 BPF
GA2	940mV/528uV	1.03	1kΩ trimpot
A8	972mV/547uV	1	Beckamn Power Amp-Helipot 823
X4	972mV/547uV	0.82	41kΩ impedance match
F7	797mV/448uV	2.24	Comstron-SEG-FA2594
GA3	1.79V/1.01mV	0.54	1kΩ trimpot
OUTPUT	5.83V/3.3mV		

TABLE VII

50 kHz FILTER BANK
GAIN/LEVEL CALCULATIONS

$$A_v = \frac{v_o}{v_i} = \sqrt{20}\ (\log_{10}^{-1}\left[\frac{6}{20}\right]) = 2.24$$

The potentometers are used to fine tune the gains of each branch. Voltage gain through each branch of the filter bank is one (0 dB).

C. LIMITER/COMPARATOR

The Plessey Semiconductor SL1624C multimode detector is used as the limiter for the PLL portion of the receiver. Its use is described in Ref. 11. The limiter output is converted by an NE527 comparator to TTL levels for use in the digital signal processor (see III). The circuit is illustrated in Figure 12. The diodes connected to the limiter input served as a pre-limiter for large signals since the maximum input to the limiter is approximately 1.5 Vnms. Care needed to be taken in this section of the circuit to prevent oscillations, since the limiter has a wideband gain of 70 dB, and the succeeding digital circuitry would be working with twice and four times the signal frequency of 50 kHz. Also the input for the X-Y Display Driver is taken from this point, to be cabled to a different rack location, and so subject to RFI. All input/outputs are differently connected where possible and leads are kept as short as possible.

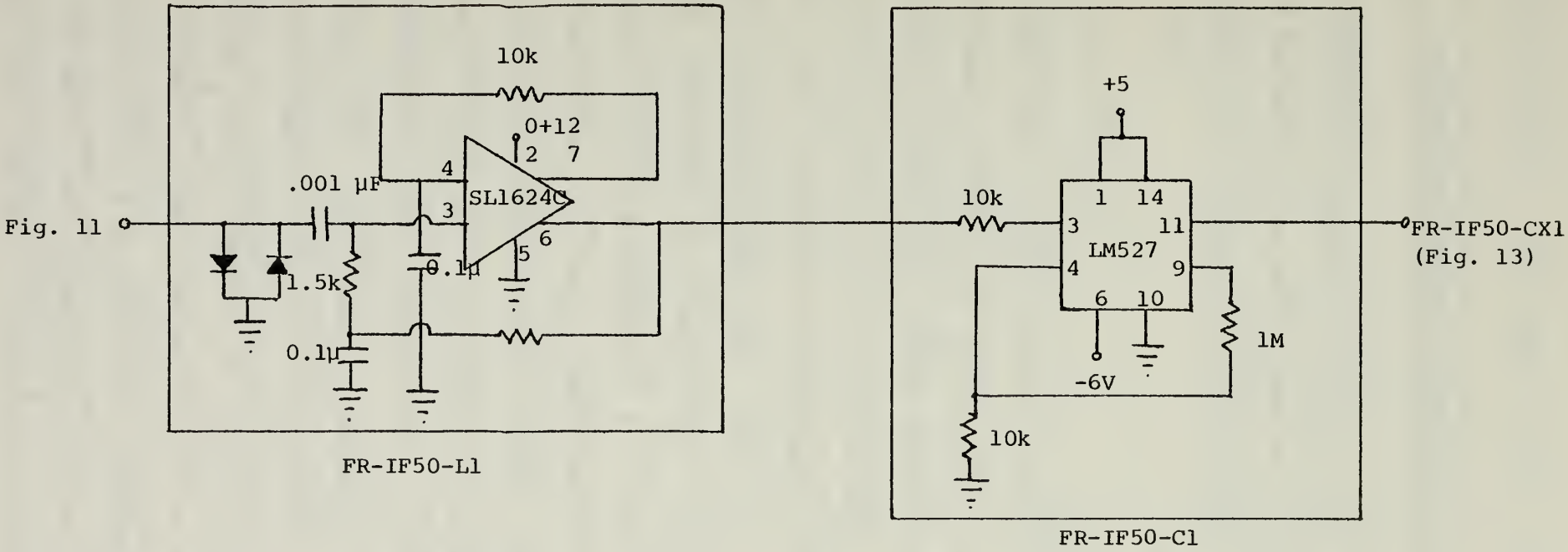


Figure 12

Limiter/Comparator Circuit

IV. 50 kHz DIGITIZED SIGNAL PROCESSING

This portion of the receiver processes frequency information only. The signal, now amplified and converted to TTL levels is digitally manipulated to extract the carrier, and drive the loop filter.

A. CARRIER EXTRACTION

Three types of signals received are of particular interest; CW, PSK, QPSK. In CW the carrier is already present and requires no further processing other than amplification and filtering. PSK and QPSK do not normally have carrier components and are typically processed in squaring loops, or quadrupling loops [Ref. 12, 13]. The same principles were employed in this circuit. PSK signals (in TTL form) are doubled in frequency, resulting in a non-phase shifting frequency component at about 100 kHz. QPSK signal is quadrupled and divided by four. The circuit is an adaptation of a frequency doubler (pg. 35) circuit in Ref. 14. The input signal at approximately 50 kHz is used to drive two 7400 NAND gate integrated circuits utilized as described. The output triggers a 74121 monostable multivibrator timed to square up the 100 kHz pulses. This in turn is used to drive a second set of 7400's and 74121 to produce a 200 kHz square wave. The 100 kHz output drives the independent flip-flop of a 74177 binary counter in a toggle configuration to divide by two. The 200 kHz output drives the other three flip-flops of the 74177 in a divide by

by four configuration. The input signal, the divided by two output, and the divided by four output are input to a 1 of 4 decoder which is used to select the CW, PSK, or QPSK mode of operation respectively. The logical circuit presentation is illustrated in Figure 13. The circuit board layout is illustrated in section VIII.C., as part of the Digital Signal Processor board.

B. EXOR PHASE DETECTORS

In an analog PLL a mixer or an AVM (analog voltage multiplier) is used as a phase detector [Ref. 4, 5]. In a digital PLL an EXOR gate can be used [Ref. 5, 15]. An in depth explanation is available in the references. However, consider an EXOR gate. When the two inputs are exactly the same frequency and 90^{o} out of phase, the output is a TTL square wave at twice the frequency of the input. This output is AC coupled and integrated through the loop filter to produce the VCXO control voltage (see V). As the signal leads or lags the reference input then the AC coupled EXOR output becomes more positive or negative, which through the integrator (and loop filter) changes the VCXO frequency and corrects the signal phase. This is how one EXOR gate is used in the frequency receiver. A second 50 kHz reference signal lagging the first by 90^{o} (para. C.) is mixed with the signal in a second EXOR gate (so that its output is all positive during lock) to act as the in lock detector. As such the first EXOR gate is referred to as the phase detector (because it's output drives the loop) and the second EXOR gate as the coherent detector

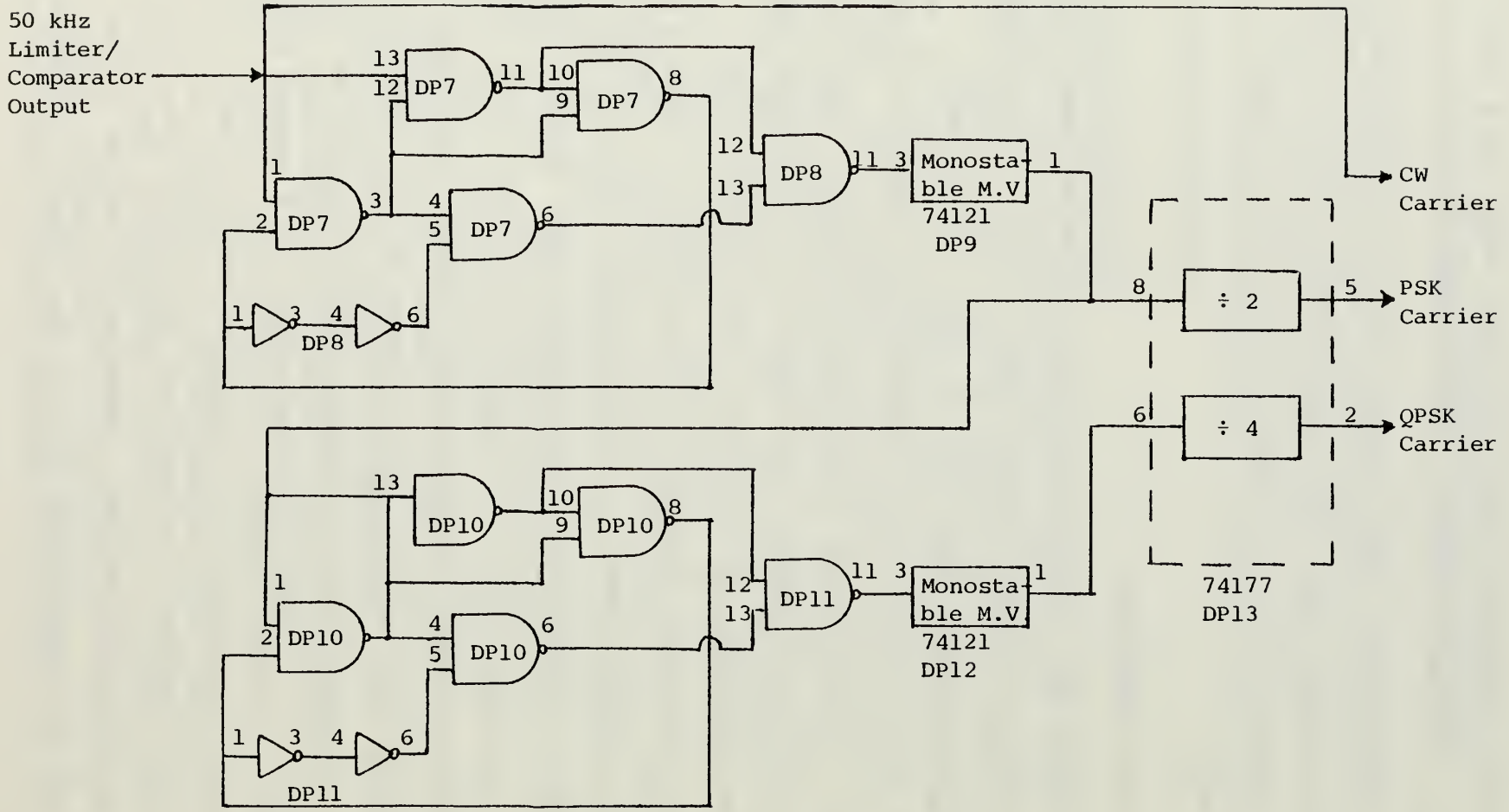


Figure 13

Carrier Extraction Block Diagram

(inputs are in phase). The circuit is illustrated if Figure 14.

To provide the greatest loop stability and accuracy it is important to ensure that the output levels of the EXOR gates remained stable. Reference 16 specifies V_{OH} of a TTL integrated circuit to be 2mV/^{o}C. This was considered acceptable. To further ensure stability all TTL loop circuitry is laid out on one printed circuit board and the 5 volt power supply for the TTL circuitry locally regulated (in the frequency receiver). This includes the carrier extraction circuits and the 50 kHz reference frequency generator.

The performance of the EXOR gates as phase detectors in the presence of noise was also considered. Reference 15 deals directly with this. Four types of phase detectors were considered, based upon their response curve of output versus phase difference of the inputs. They are sinusoidal, triangular, saw tooth, and bang-bang (Figure 15). The phase detectors in the A6 receiver were sinusoidal, and the EXOR's are triangular, so only their performance is tabulated. Two criteria were considered; first, the degradation in signal to noise ratio (noise figure) was determined, and second, degradation in signal to noise spectral ratio was determined. The reference (0 dB degradation) was an ideal multiplier (Figure 16a). The noise figure results are tabulated for the two types of detectors in Figure 16b, 16c for low signal to noise ratio inputs. The results were independent of the BPF in the phase detector input. The signal to noise spectral ratio results are tabulated in Figure 16b and 16c also, and here the type of BPF used in the

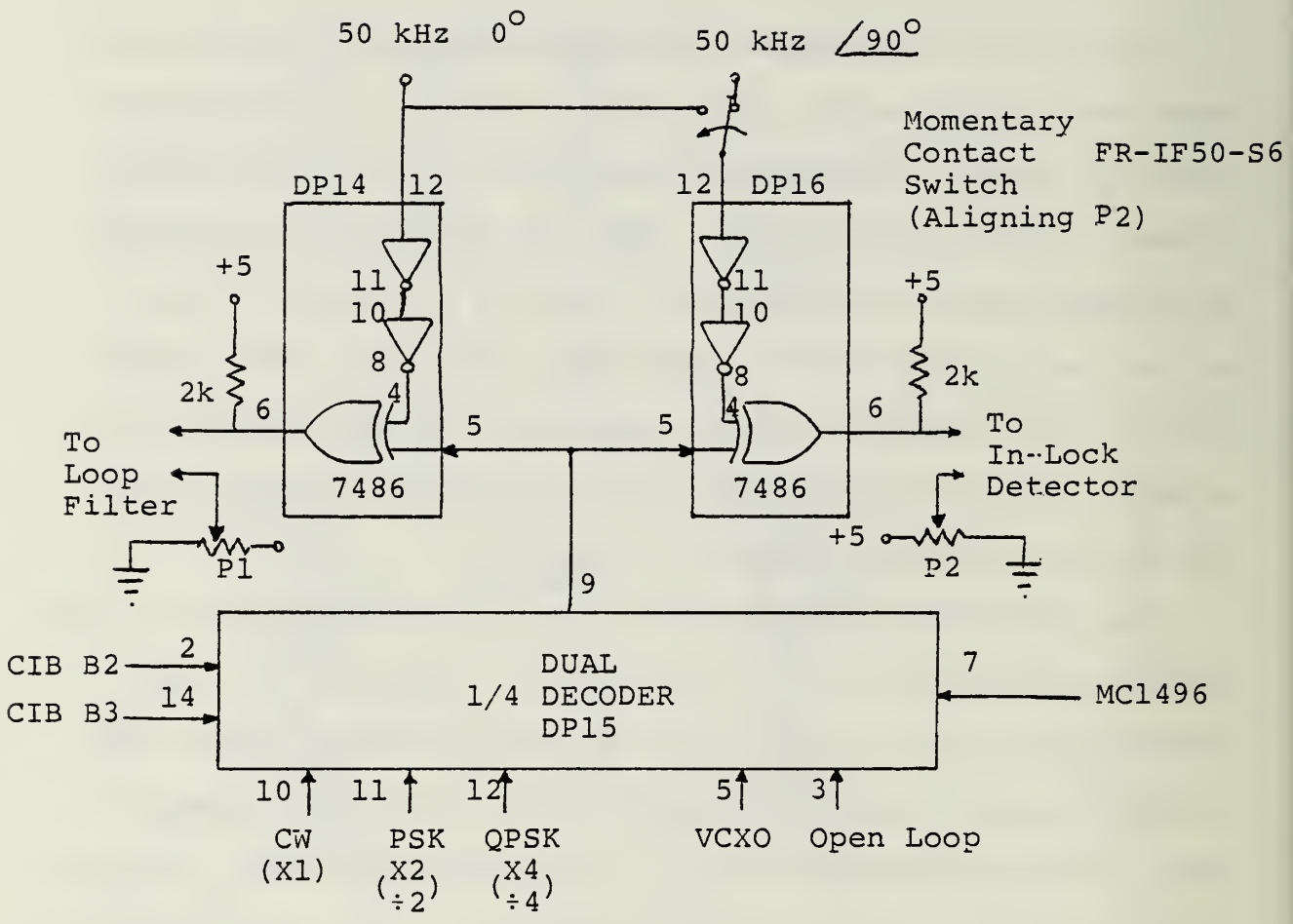


Figure 14

EXOR Phase Detectors

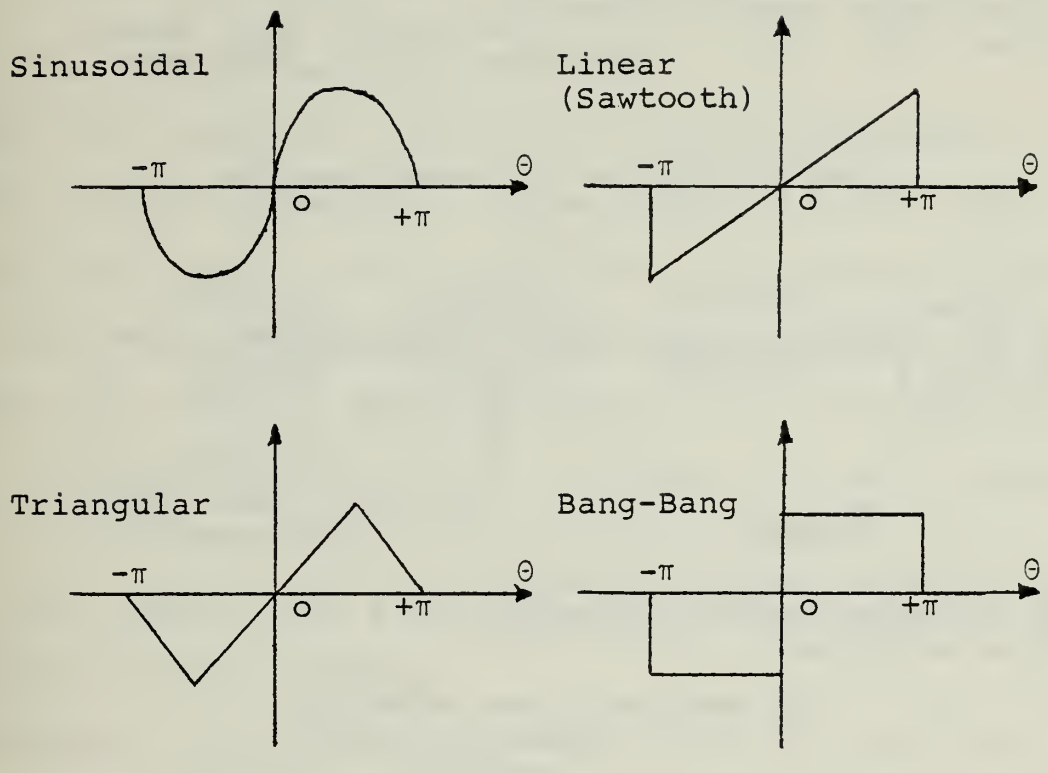
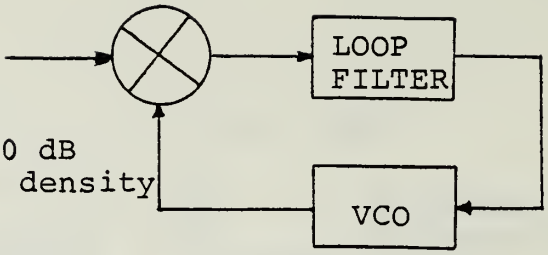


Figure 15

Phase Detector Characteristics

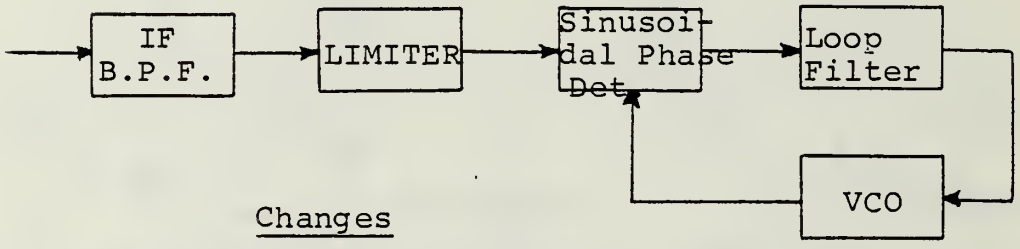


Changes

Signal to Noise ratio = 0 dB
Signal to Noise spectral density
ratio= o dB

Ideal Multiplier As Phase Detector

(a)

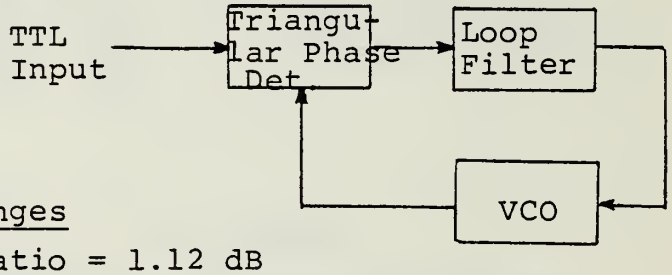


Changes

Signal to Noise ratio = -1.05 dB
Signal to Noise spectral density
ratio= -0.65 dB

Sinusoidal Phase Detector

(b)



Changes

Signal to Noise ratio = 1.12 dB
Signal to Noise spectral density
ratio= -0.70 dB

Triangular Phase Detector

(c)

Figure 16

Phase Detector Performance

phase detector input does affect the results. The difference in performance was considered acceptable to obtain the easier design facilitated by using digitized signal processing.

C. 50 kHz REFERENCE SIGNAL GENERATOR

The final section of the Digital Signal Processor was the 50 kHz reference generator. As mentioned in B, two reference signals are required for the EXOR phase and coherent detectors. The first must always lead the second by 90 degrees, so that, in lock, the coherent detector output is at a TTL high level (5V). A circuit using two J-K flipflops in a ring configuration, as described in Ref. 14 is used to generate such a pair of 50 kHz signals from a reference 200 kHz generated in the Frequency Unit of the SSA.

A second set of 50kHz signals that leads the first set is needed for the X-Y display (see section VI), to compensate for phase lag of the signal thru the limiter/comparator and carrier extractor. This second set is generated using the same scheme used for the first set, only the 200 kHz reference is first passed through a 74121 monostable multivibrator to vary the trailing edge of each pulse. The J-K flip-flops are trailing edge triggered. In this way the 200 kHz reference edge is varied through 360 degrees of phase, resulting in 90 degrees of phase adjustment at 50 kHz.

To ensure that the second pair of 50 kHz signals always led the first by a variable amount from 0 to 90 degrees, as

shown in Figure 17, some EXNOR and NOR logic was added. Without it the phase relationship between the first and second set of 50 kHz references is a nominal value $\pm$ 90 or + 0 or + 180 degrees depending upon start up conditions of the independent J-K flip-flop pairs. Referring to Figure 17a it was observed that when all the signals are in their proper phase configuration, if W and X are not the same logical level, then W and Y are the same logical level. If this were not true then a control D-type flip-flop (7474) is cleared. This output is used to drive the clear input of the J-K flip-flops for the X-Y display set of 50 kHz references low, thus clearing all output of this set. When conditions are correct (W and X both logical zeros) (Fig. 19b) then the control flip-flot Q output is set high using the pre-set, which allows the second J-K flip-flop set to begin operation. The control logic is shown in Figure 18 along with the complete 50 kHz reference signal generator.

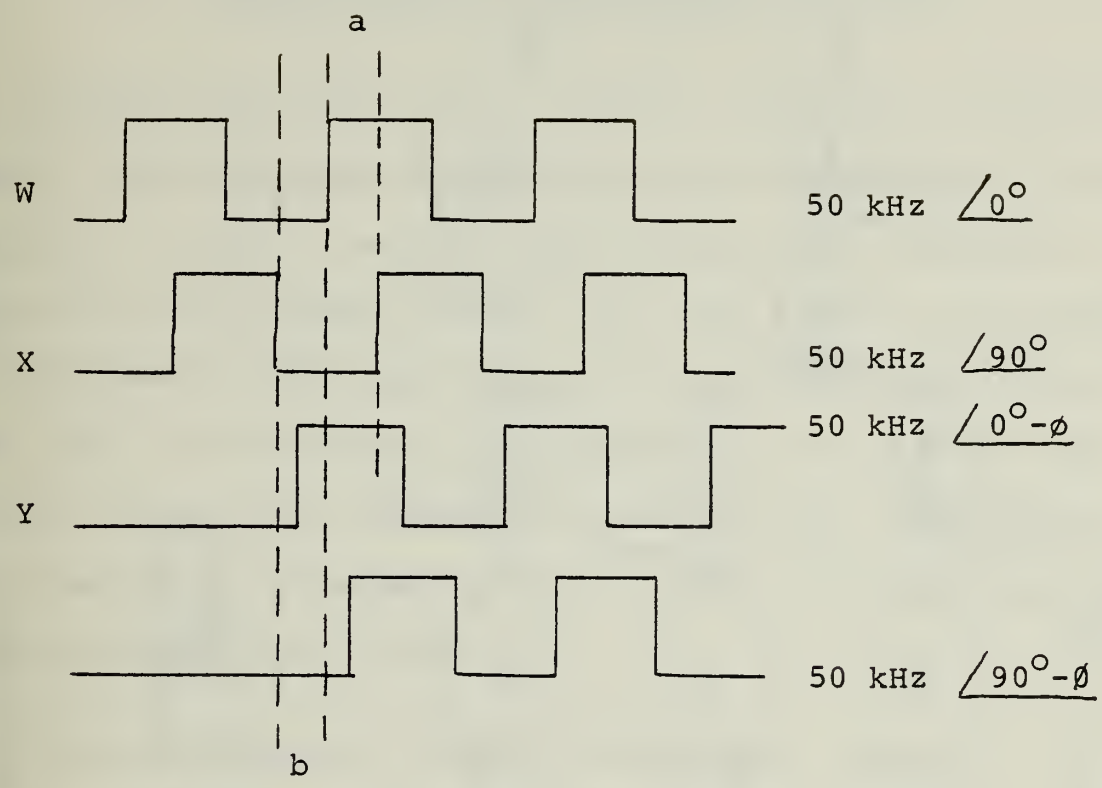


Figure 17

50 kHz Reference Frequency Phase Relationships

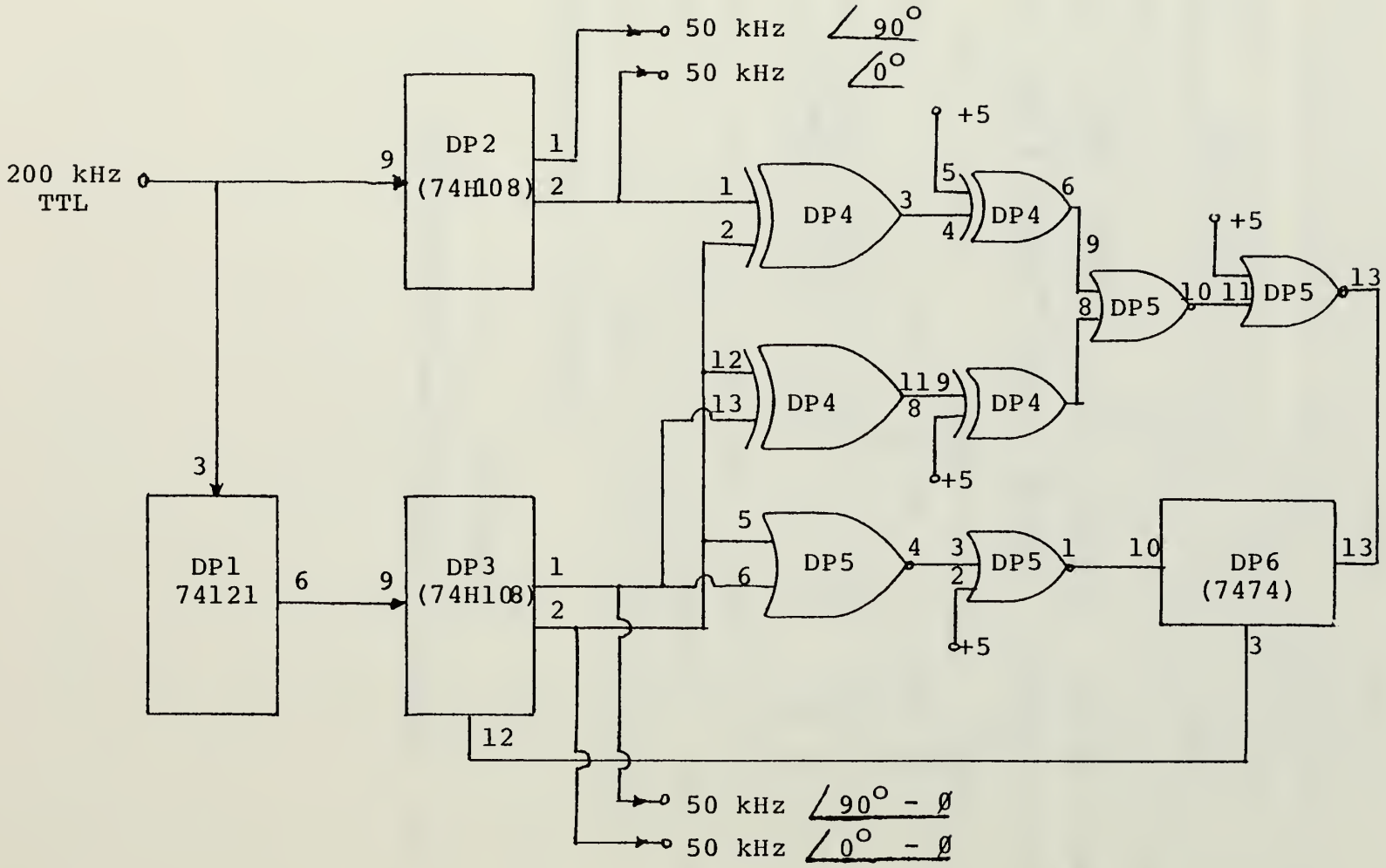


Figure 18

50 kHz Reference Frequency Generator (FR-IF50-RF1)

V. PHASE LOCKED LOOP-FREQUENCY TRACKING

Although this part of the receiver could be considered the heart of the receiver, the complications of designing the IF sections (29 MHz, 1 MHz, 50 kHz) consumed a considerable majority of the design effort. For this reason a firm design for the loop filters was not completed. Much work was done on this part of the receiver, particularly in specifying the Voltage Controlled Crystal Oscillators (VCXO), and considering the feasibility of sweeping the VCXO's for faster acquisition. These considerations follow.

A. VOLTAGE CONTROLLED CRYSTAL OSCILLATORS

The A6 receiver (paragraph I.A.) was the test bed for determining the VCXO parameters for the frequency receivers. The center frequency (950 kHz) was kept, because it was low enough to result in sufficient significant digits of frequency measurement on the HP5345A counter (± 0.0001 Hz for 1.0 second gate time). The 50 kHz frequency that resulted from the 950 kHz mixing with 1 MHz was also found to be a reasonable frequency for designing hardware. The frequency control range was chosen as ± 2 kHz. The A6 receiver VCXO's have control ranges of ± 190 Hz, ± 950 Hz, and ± 9.5 kHz. The ± 190 Hz range would not be useful in the frequency receiver. It found little use in the A6 receiver. The ± 950 Hz rnage found the most general use, but was too narrow considering a ± 1 kHz transmitter specification /Table I/.

The ± 9.5 kHz range was larger than needed in nearly all cases, and made narrow loop filter design difficult due to its frequency versus control voltage characteristic. Also only one (vice 3) VCXO was chosen, the ± 2 kHz range being sufficient to track transmitter drift (± 1 kHz), and still enable sufficiently narrow loop filter design (20 Hz). Stability specifications were set at ± 50 Hz to ensure accuracy, and minimum drift with temperature and time. Voltage levels were chosen to conform with anticipated available levels (± 12, 5 VDC).

B. SWEEPING THE VCXO

Sweeping the VCXO in a PLL is considered in Ref. 17. That reference illustrates the circuitry used in that application.

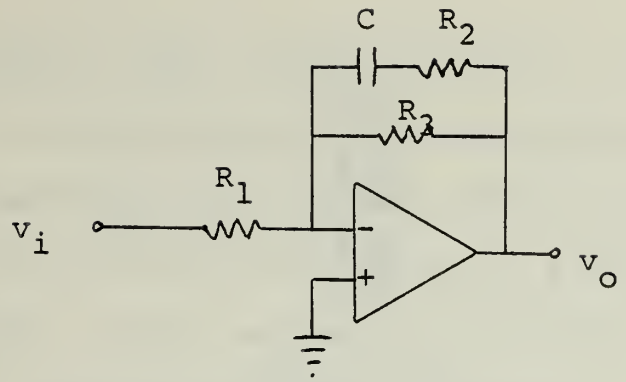
Maximum sweep rates were empirically obtained and validated the theoretical sweep rates derived in Ref. 4.

C. LOOP FILTER

The desired loop filter has an imperfect second order transfer function (paragraph I.B.). Two schemes were considered (Figure 19). Neither was brought to a final design, but are included to facilitate their design in continued frequency receiver development. Loop filter bandwidths of 20 Hz, 100 Hz, 300 Hz, and 1000 Hz were considered desirable.

D. OPEN LOOP OPERATION

This circuit was designed to operate the receiver in an open loop mode (Figure 20). In this mode an external frequency source, the test unit Rockland Synthesizer 5610A, is used to approximately lock up the receiver by replacing the VCXO to



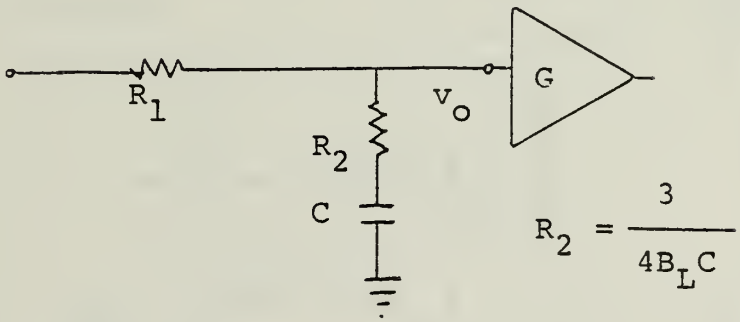
$$F(\ ) = \frac{R_3(R_2+1/CW)}{R_1(R_2+R_3+1/CW)} = R\frac{1 + j\tau_2\omega}{1 + j\tau_1\omega}$$

$$R = R_3/R_1$$

$$\tau_1 = C(R_2+R_3)$$

$$\tau_2 = R_2C$$

IMPERFECT SECOND ORDER TRANSFER FUNCTION - ACTIVE ELEMENTS



IMPERFECT SECOND ORDER TRANSFER FUNCTION - PASSIVE ELEMENTS

FIGURE 19

LOOP FILTER CIRCUITS

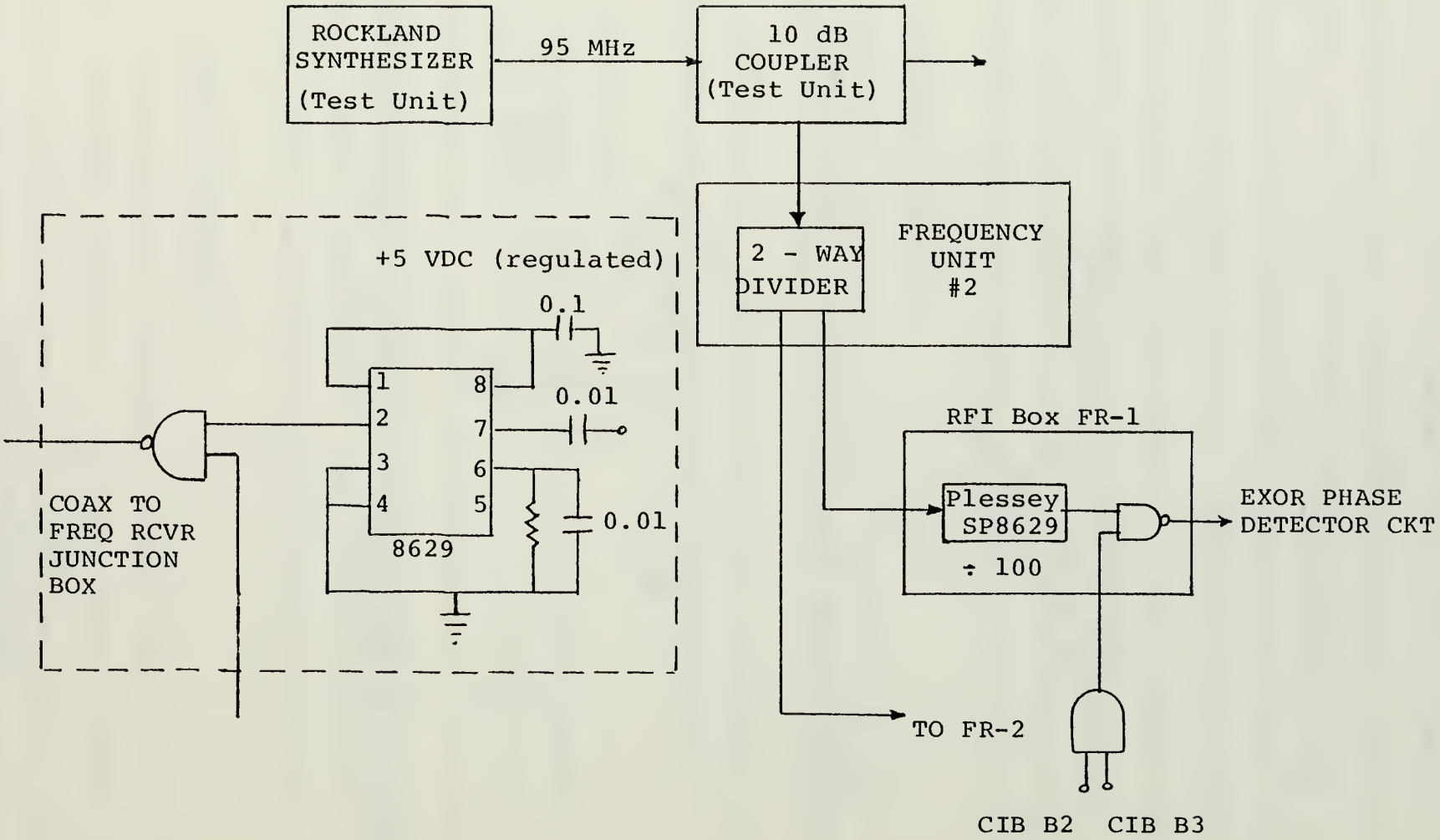


FIGURE 20

OPEN LOOP CONTROL

drive the carrier input terminals of M3. In this way phase modulation of received signals can be observed on the X-Y display if the frequency is tuned close to the signal input frequency (Δf = 0.1 Hz would result in X-Y display rotation of 36^{o}/second). Tuning steps of 0.1 Hz are achieved by dividing the synthesizer output, nominally tuned to 95M Hz, by 100 and stepping the synthesizer in 10 Hz steps. Output level of the synthesizer is set to +13 dBm. A Plessey Semiconductor SP8629 /Ref. 22/ is used to implement the divide by 100 with one component. It required 200 mV p-p to 1000 mV p-p sinusoidal input, and the synthesizer level is within this range after coupling and dividing as shown in the figure. The insert illustrates the proper SP8629 pin connections as described in the reference.

VI. X-Y DISPLAY

A. EXPLANATION OF THE DISPLAY

The X-Y display is a standard X-Y oscilloscope. To illustrate how the X and Y inputs are derived and why the frequency receiver is used to drive the display the simplest case is considered. Assume a CW input signal to the receiver. After synchronous mixing by the frequency receiver's PLL the output is

$$A \cos 2\pi(50\text{x}10^3)t. \qquad (1)$$

Consider the X input as the product of (1) and the 50 kHz reference signal into the phase detector[1]

$$A \cos 2\pi\ (50\text{x}10^3)t \cos\{2\pi(50\text{x}10^3)t + 0^o\} = 1/2A \qquad (2)$$

(after filtering the 100 kHz component).

And similarily consider the Y input as the product of (1) and the 50 kHz reference into the quadrature detector

$$A \cos 2\pi\ (50\text{x}10^3)t \cos\{2\pi(50\text{x}10^3)t + 90^o\} = 0 \qquad (3)$$

(ignoring the 100 kHz components).

Equations (2) and (3) assume that the CW signal is exactly in

---

[1] For simplicity the 50 kHz reference is shown as a pure sine wave, when in fact it is a TTL square wave. Filtering the harmonics out of the product of the CW input and a square wave will yield the same result.

phase with the references. However, there is a phase shift since the X-Y display signal is pulled off prior to the limiter. The shift is equal to the phase shift caused by the limiter/comparator and the carrier extractor. Equation (2) then becomes

$$A \cos 2\pi (50\times10^3)t \cos\{2\pi(50\times10^3)t + 0^\circ - \phi\} = 1/2\ A \cos \phi \quad (4)$$

and (3) becomes

$$A \cos 2\pi(50\times10^3)t \cos\{2\pi(50\times10^3)t + 90^\circ - \phi\} = 1/2\ A \sin \phi \quad (5)$$

From this it can be observed that the Y input increases and X input decreases. Depending upon the phase shift (ϕ) the CW X-Y presentation could be off from the vertical by as much as 20 or 30 degrees ($\phi=20^\circ$-30°). It is desired to have the normal displays oriented on the vertical and/or horizontal axis. This is why the 50 kHz references for the X-Y display driver can be phase shifted (paragraph IV.C.). Similar calculations can be done with PSK,

$$PSK = A \cos\{2\pi(50\times10^3)t + \theta\};\ \theta=\phi,\ \phi + 180^\circ \quad (6)$$

and QPSK

$$QPSK = A \cos\{2\pi(50\times10^3)t + \theta\};\ \theta=\phi,\ \phi \pm 90^\circ,\ \phi + 180^\circ \quad (7)$$

and are left to the reader. Similarly it could be readily shown that if the reference signals (50 kHz, TTL) are not "locked" in phase with the signal then the X-Y display vectors will rotate on the scope. A PLL implementation is thus desirable.

B. DISPLAY DRIVER/CONTROLLER

Two functions are performed by the X-Y Display Drive Circuit. This first is to implement the X-Y inputs as described in A. The second is to scale the inputs to match the fixed volts/division setting of the oscilloscope, since input signal levels can vary over 65 dB in a selected range. The circuit in Figure 21 does this. The calibrated voltage level of either Frequency Receiver 1 or 2 is selected by FR-IFXY-S1, an analog switch. Both operational amplifiers of a TL083CN dual op amp chip are configured about discrete gain steps, the first to buffer the input, and the second to amplify (A_V=7.713) the attenuated input signal to be at or near full-scale deflection on the oscilloscope. Since the inputs from the frequency receivers are calibrated, use of 1% resistors for the steps of the attenuator section gave an accurate ($\pm$ .25 dB $\pm$ 2%) signal power level of what full-scale X-Y display deflection actually is.

The additional percent is contributed by the analog switch resistance. This error is minimized by keeping the values of the attenuator resistors high. If R_s = Switch Resistance and $R_\#$ = attenuator resistor in Figure 21 then:

$$\text{Attenuation} = \frac{R_\# + R_s}{R_\# + 6\ M\Omega + R_s}$$

$$\text{error} = \frac{R_s}{R_\#}$$

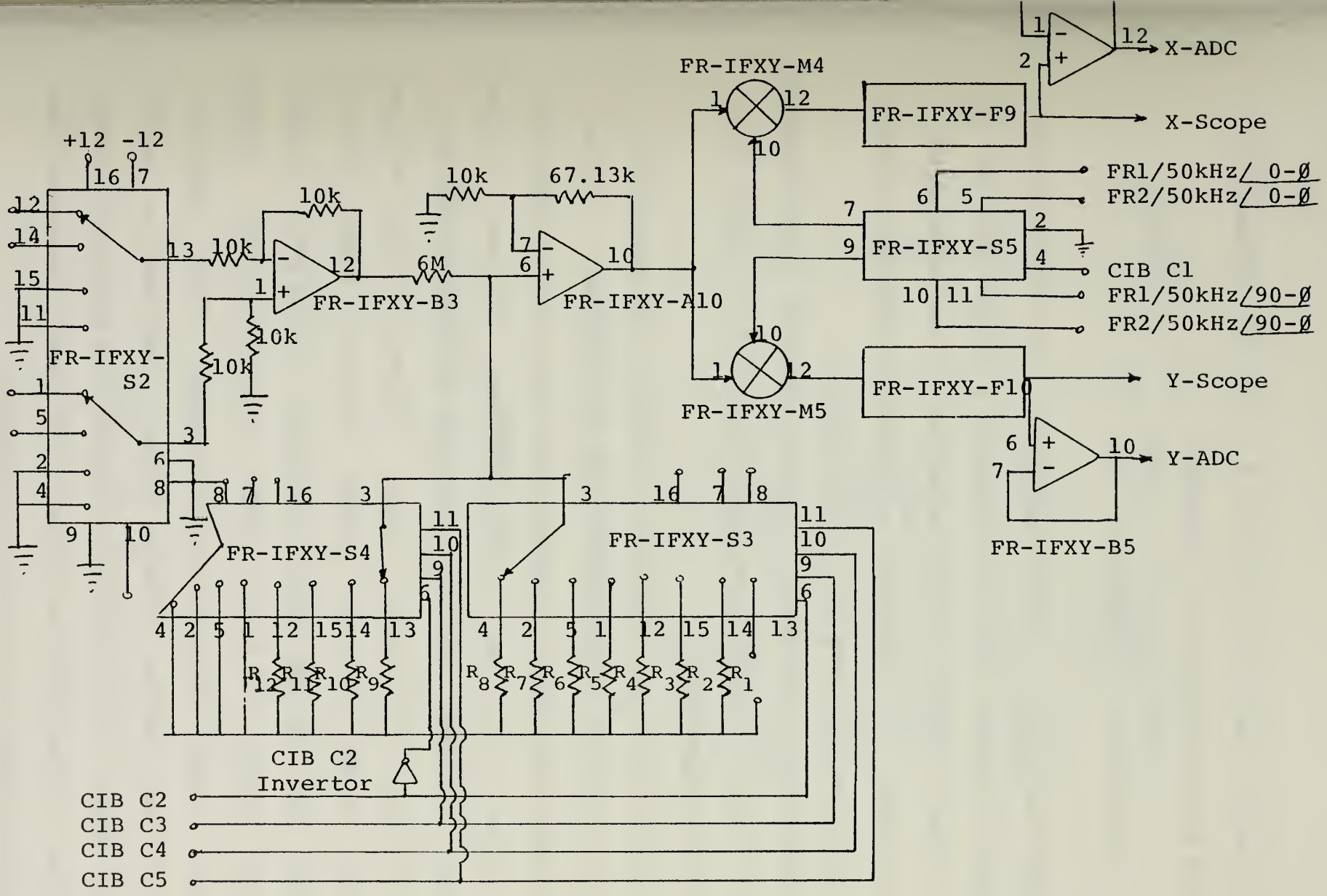


FIGURE 21

X-Y DISPLAY DRIVER

Maximum error occurs with minimum $R_{\#}$ = 10.82k (Table VIII). R_s could be as high as 120, therefore,

$$\text{error/max} = \frac{120}{10.82k} = 1.1\%$$

The amplifier output is then connected to two MC1496 analog voltage multipliers (AVM), one for the X channel and one for the Y. Their outputs in turn go through a low pass filter, with a DC bias, to remove sum and harmonic frequency terms, and the DC level in the AVM output (9VDC).

Additionally, a buffered input is provided to be connected to the X-Y ADC to enable computer production of a hard copy of the X-Y presentation.

The gain steps are determined based on the selections that would be made available for the SSA operator. In the SATCOM range maximum X-Y display deflection can be selected for a signal of -85 dBm, -90 dBm, -95 dBm, -100 dBm, -105 dBm, -110 dBm, -115 dBm, -120 dBm, -125 dBm, -130 dBm, -135 dBm, and -140 dBm. In the RFI -2 range, -50 dBm, -55 dBm, -60 dBm, -65 dBm, -70 dBm, -75 dBm, -80 dBm, -85 dBm, -90 dBm, -95 dBm, -100 dBm, and -105 dBm can be selected. In the RFI -1 range, -20 dBm, -25 dBm, -30 dBm, -35 dBm, -40 dBm, -45 dBm, -50 dBm, -55 dBm, -60 dBm, -65 dBm, can be selected. This, combined with the known posible voltage levels at the input to the X-Y display deiver (3.3m Vrms to 5.83 Vrms) and the desired maximum input to the MC1496 multipler (≈80m Vrms) determined the attenuation steps illustrated in Figure 21.

(dB) ATTENUATION	RATIO	(Ω) RESISTANCE
0	1	$R_1 = \infty$
5	0.56	R_2 = 7.636M
10	0.32	R_3 = 2.824M
15	0.18	R_4 = 1.317M
20	0.10	R_5 = 667k
25	0.056	R_6 = 356k
30	0.032	R_7 = 198k
35	0.018	R_8 = 110k
40	0.010	R_9 = 60.61k
45	0.0056	R_{10}= 33.79k
50	0.0032	R_{11}= 19.26k
55	0.0018	R_{12}= 10.82k

Gain at 0 dB attenuation = 7.713

TABLE VIII

RESISTOR VALUES FOR THE X-Y DISPLAY DRIVER

The inhibit control input of S2 and S3 is used to allow control with four bits. If operated separately they would require six control bits. The truth table is illustrated in Table XII.

The X-Y Display Driver is not located with the frequency receivers, but mounted in the X-Y display chasis. Interconnections to it from the frequency receivers, since either one can be chosen to drive the X-Y display, are made through the Frequency Receiver Interconnection panel (see Table X). Output to the X-Y analog to digital converters is directly from the X-Y chasis, and not through the Interconnection Panel (paragraph VII).

	ITEM	QUANTITY
IC's	RCA CD4052BE	2
	RCA CD4051BE	2
	74153	1
	TI TL083CN	2
	MC 1496	2
	DATEL FLT-U2	2
	7404	1
ESISTORS	TABLE VIII 1% RESISTORS	12
	10K	7
	67.13k	1
	6M	1
	1k	8
	3k	6
	1.5k	2
	820	2
	100	2
CAPS	1.0μ	10
	0.1μ	1
	0.001μ	4

TABLE IX

PARTS LIST FOR X-Y DISPLAY DRIVER

VII. FREQUENCY RECEIVER INTERCONNECTION PANEL

To simplify, and organize the cabling to and from the frequency receivers and X-Y Display, a distribution panel is used. This permits the use of one cable to each receiver carrying all control data, reference frequencies, and status lines. The routing is shown in Figure 23, and a list of inputs, outputs, and interconnects in Table X. Different type connectors are used for each I/O type, to prevent inadvertent wrong connections. In all, 4 types of connectors were required; one type for the CIB's, one for the Frequency Receivers, one for the CPU, one for the X-Y Display Driver.

FROM \ TO	FR1	FR2	X-Y DISPLAY DRIVER	CPU
FR 1/2 CIB	16 bits (Fig.24)	16 bits (Fig.24)		
X-Y CIB			5 bits (Table XI)	
FR1			amplified/filtered signal/50 kHz ref. frequencies	in/out lock
FR2			amplified,filtered signal/50 kHz ref. frequencies	in/out lock

TABLE X

INTERCONNECTION BUS DATA FLOW

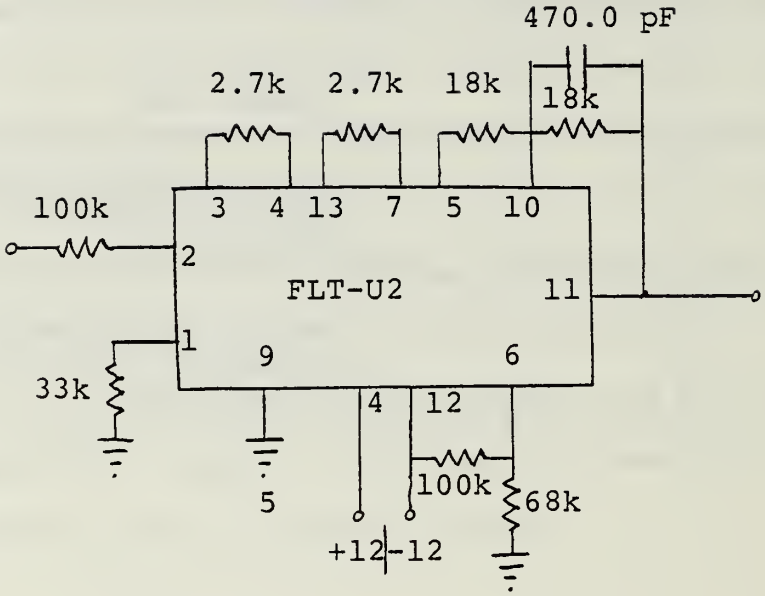


Figure 22

FR-IFXY-F9/F10

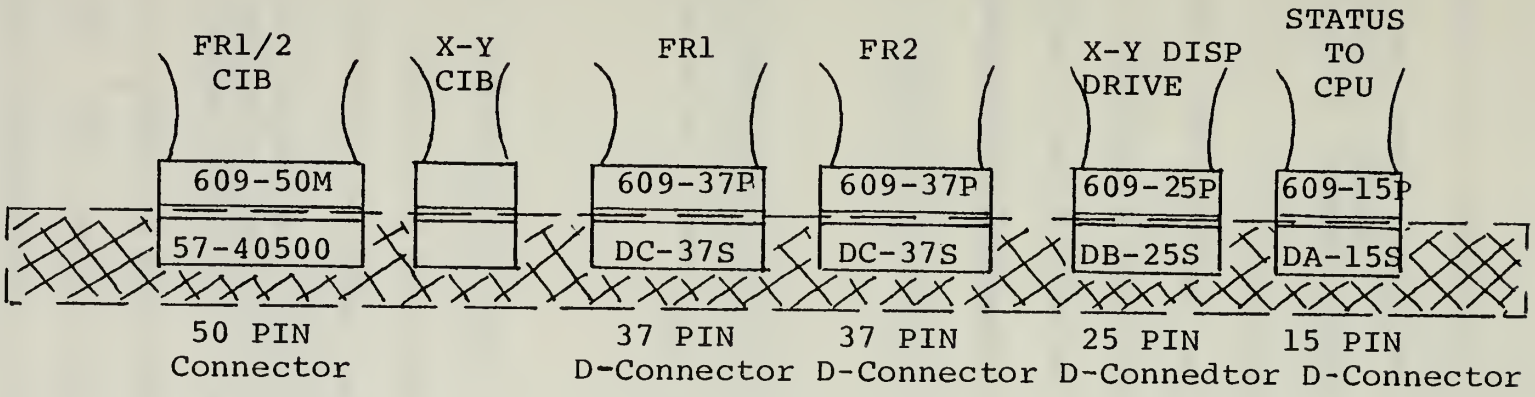


Figure 23

Interconnection Panel
(Mounted to Rack Frame)

VIII. SPECIFIC USER SECTIONS

This section is intended to facilitate the incorporation of the frequency receivers into the SSA. Data pertinent to software control development, layouts needed for receiver production, and procedures for adjusting and calibrating the receiver are presented. Some redundancy of the information presented in earlier sections could not be helped and is intentional. This section is intended to be an assimilation of data for specific users, not necessarily interested in the design development presented in earlier sections.

A. COMPUTER CONTROL

Software development is divided into what the receiver requires from the computer, and what data the receiver will be feeding to the computer.

1. Input (Control)

The frequency receivers were designed for computer control. There are no manual controls available to the operators, and there is no manual mode of operation. The two frequency receivers of the SSA share one Control Interface Board (CIB) /Ref. 23/, with the X-Y display control bits on a separate CIB. The control functions of each bit or bit group is shown in Figure 24, Table XI and XII. The display of control functions available to the operator and the desired bit output for each function is shown in Figures 25 and 26. Control of the Rockland Synthesizer /Ref. 18/ that tunes the

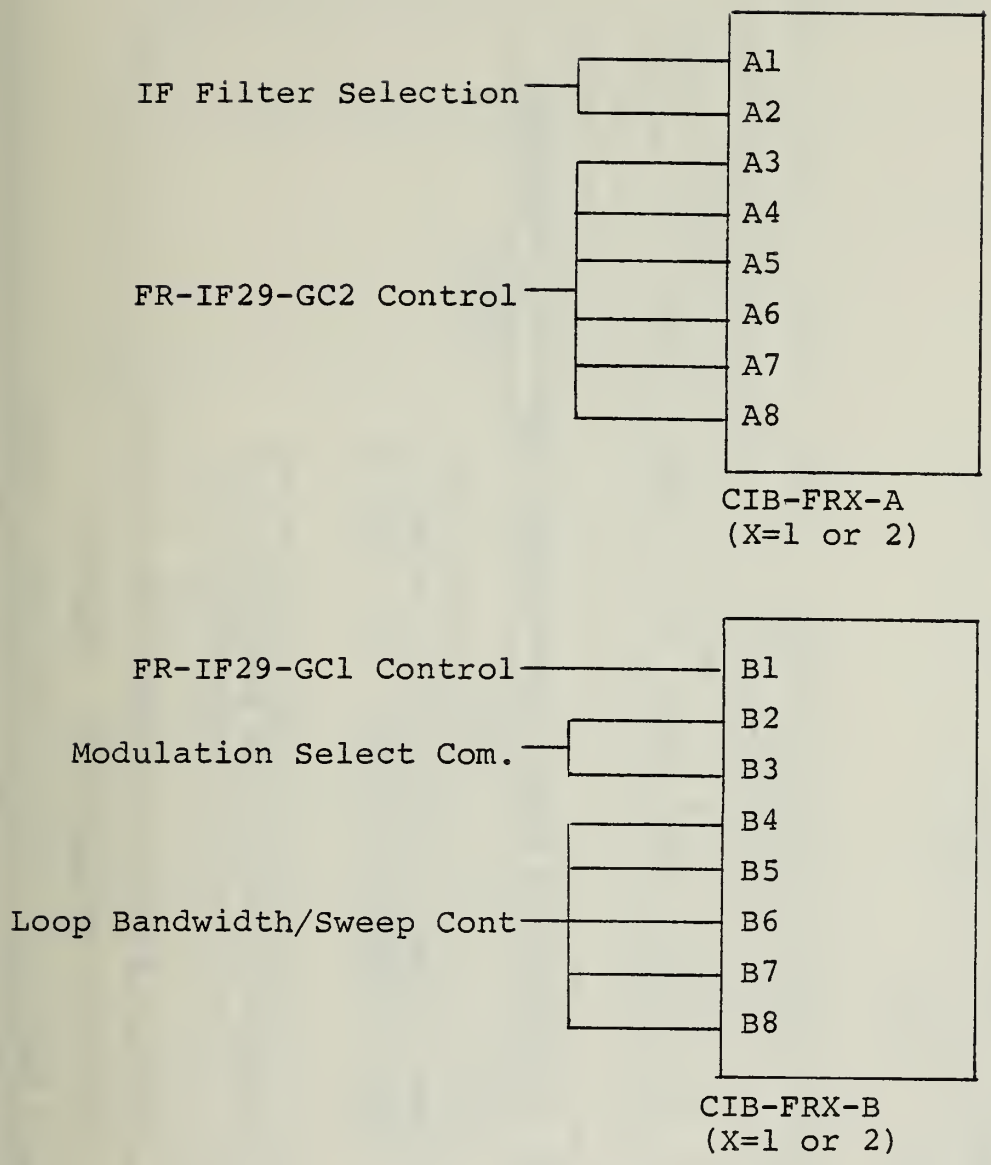


Figure 24

Frequency Receiver CIB Distribution

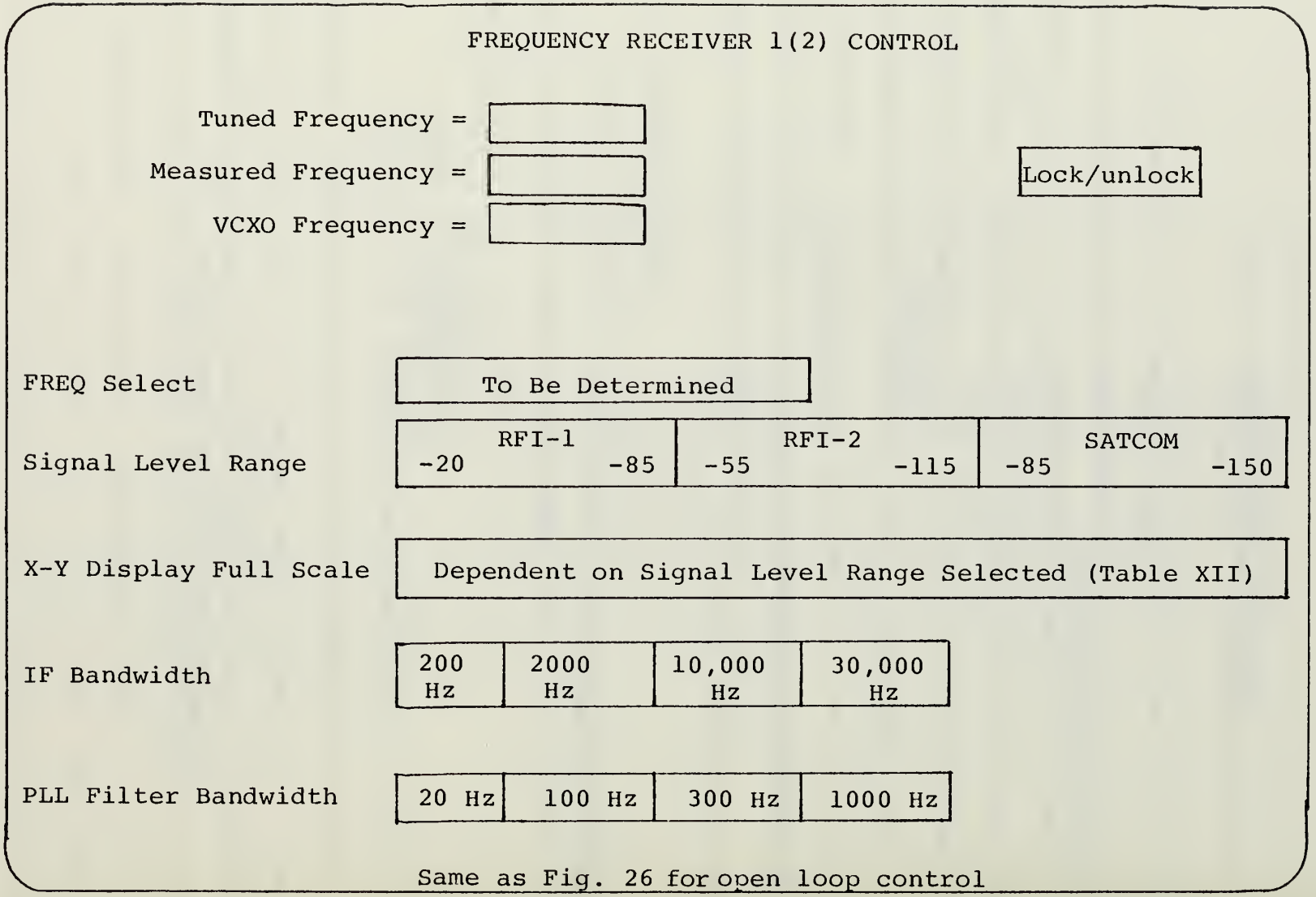


Figure 25

Frequency Receiver - Trouble Shooting Control

FREQUENCY RECEIVER 1(2) CONTROL

Tuned Frequency = [ ]

Measured Frequency = ["Receiver out of lock"[1]]

Frequency Select [To Be Determined]

Signal Level Range

RFI 1	RFI 2	SATCOM
-20 -25	-55 -115	-85 -150

X-Y Display Full Scale [Dependent Upon Signal Level Range (Table XII)]

Signal Type

75b/s	300b/s	600b/s	1.2b/s	2.4b/s	4.8b/s	9.6b/s	19.2b/s	32b/s

Open Loop Enable [ON] [OFF]

X-Y Synchronization

Down/Fast	Down/Slow	Nominal Freq. Reset	Up/Slow	Up/Fast

Nominal Reference Freq=950kHz

1. Frequency reading from the HP5345A could be voided from this display and this warning substituted.

Figure 26

Frequency Receiver - Normal Control

			A1	A2
IF FILTER SELECTION	30 kHz B.W.		0	0
	10 kHz B.W.		0	1
	3 kHz B.W.		1	0
	200 kHz B.W.		1	1
			IN	OUT
FR-IF29-GC2 CONTROL	32 dB	A3	1	0
	0.5 dB	A4	1	0
	1.0 dB	A5	1	0
	2.0 dB	A6	1	0
	4.0 dB	A7	1	0
	8.0 dB	A8	1	0
FR-IF29-GC2 CONTROL	32.0 dB	B1	1	0
			B2	B3
CARRIER MODULATION/ OPEN LOOP/CONTROL	CW/Closed Loop		0	0
	PSK/Closed Loop		0	1
	QPSK/Closed Loop		1	0
	/Open Loop		1	1

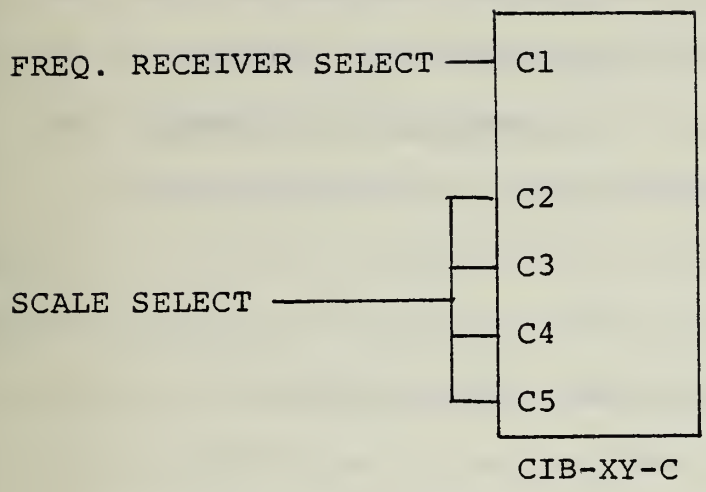
LOOP FILTER B.W./VCXO SWEEP CONTROL (to be determined at a latter date)	B4	B5	B6	B7	B8
	X	X	X	X	X

FREQUENCY RECEIVER CIB CONTROL FUNCTIONS

RANGE	SETTING
RFI-1	B1,A3,A5 = 1,1,1
RFI-2	A3,A5,A6 = 1,1,1
SATCOM	A5,A7 = 1,1

NOMINAL SETTINGS FOR RANGES (no calibration)

TABLE XI



FREQUENCY RECEIVER SELECT				C1			
			FR1	0			
			FR2	1			
	SATCOM	RFI 2	RFI 1	C2	C3	C4	C5
	-140	-110	-65	0	0	0	0
	-135	-105	-60	0	0	0	1
	-130	-100	-55	0	0	1	0
	-125	-95	-50	0	0	1	1
	-120	-90	-45	0	1	0	0
	-115	-85	-40	0	1	0	1
	-110	-80	-35	0	1	1	0
	-105	-75	-30	0	1	1	1
	-100	-70	-25	1	0	0	0
	-95	-65	-20	1	0	0	1
	-90	-60		1	0	1	0
	-85	-55		1	0	1	1

TABLE XII

X-Y CIB DISTRIBUTION/CONTROL FUNCTION

receiver is a desirable control function to be presented with the other receiver controls, but is not included on the frequency receiver CIB, and not discussed here. Control of the Rockland Synthesizer used with the test unit to operate the receiver in an open loop mode (Figure 20) is described in paragraph I.D.

2. Receiver Outputs

Directly from the receiver are two outputs. One is a status line indicating the receiver is in lock (high) or out or lock (low). This output is to be used to validate the frequency measurement obtained from the HP counter. The second output is from the X-Y display through the X-Y display ADC's. This data is intended to be used to produce hard copies of the X-Y Display, and to calibrate the receiver (see paragraph VIII.B.2).

Two other outputs are required to be processed by the computer that are not directly available from the receiver. One is the frequency reading of the HP counter assigned to each receiver. Control and operation of the counter is covered in Ref. 19. The second is the time of counter measurement, accurate 5o $\pm$ 0.01 seconds since DAMA signal bursts are 0.1 seconds in width /Ref. 20/.

To summarize, the information required to be read and stored or processed by the computer is:

a. Rockland Synthesizer frequency setting

b. HP5345A counter reading

c. Time of reading in (b.)

d. Status of in-lock line during entire reading. (any unlock indication during the gated measurement of the HP5345A in-validates the measurement).

3. Information Processing

Since raw data is only ossasionally useful to an operator, the data output by the computer to the control console or on printed displays should be.

a. Tuned frequency = Rockland Synthesizer setting + 151 MHz

b. Measured frequency = HP counter reading + Rockland Synthesizer setting + 150.05 MHz

c. Frequency Measurement validity - voiding presentation and cueing the operator that the receiver is unlocked, if the lock/unlock line went low at a time during measurement.

d. Time of measurement.

e. Frequency Receiver used (1 or 2).

The ability to display raw data (Figure 25) is desirable only for troubleshooting.

B. INSTALLATION OF THE RECEIVER

Because receiver adjustments frequently result in erroneous operation of the receiver by the uninformed, and complicate troubleshooting for the informed, every effort was made in the design to reduce the number of adjustments. However a receiver whose output is intended to be calibrated to $\pm$ 0.25 dB cannot escape some adjustments. Nearly all of these are intended to be

made upon initial installation and remain unchanged for the receiver functional lifetime.

1. Adjustments

a. Trimpot T1 in the 1 MHz IF section adjusts the AC voltage level on pin #1 of M3 (MC1496) to 80 mVrms under the following conditions.

1) -58.5 dBm input of frequency fs to R port of M1
2) Rockalnd Synthesizer output level at +13 dBm, frequency of fs +29 MHz
3) GC1 selected to 0 dB
   GC2 selected to 5 dB

b. Trimpot T2, T3, T4 adjust the AC voltage level on pin +13 of S1 (CD4052A) as follows:

1) Select the 30 kHz IF filter
2) Record AC voltage at pin #13 on S1
3) Select the 10 kHz IF filter
4) Adjust T2 until the voltage on pin #13 of S1 is the same as in 2.
5) Select the 3 kHz IF filter
6) Adjust T3 until the voltage on pin #13 of S1 is the same as in 2.
7) Select the 200 kHz IF filter
8) Adjust T4 until the voltage on pin #13 of S1 is the same as in 2.

c. Trimpot T5 adjust the phase of the inputs to the quadrature detector. Using a dual trace oscilloscope with trace A to pin 12 and trace B to pin 5 of IC 01,adjust (Fig. 16) T5 until the two signals (50 kHz TTL) are 90^{o} out of phase.

d. Trimpot T6 adjust the threshold sensitivity of the lock detector. By reading the DC boltage level on pin 6 of connector D1 adjust the level of 0 VDC which depressing S6 (complete step c. first).

2. Calibration

In a fully operational SSA the frequency receiver can and should be calibrated to have a flat response over the frequency range of interest, 243 MHz to 270 MHz. With the receiver configured for nominal gain the input frequency is swept over the above frequency range. The computer records frequency versus level at the X channel ADC of the X-Y Display. The levels are converted to decibels, and the mean value computed. The computer can now compute how to set the calibration bits of GC2 depending upon the frequency tuned, by referring to a look-up table that contains the output level deviation from the mean.

C. RECEIVER PRODUCTION

This part is a separate list of Figures and Tables that refer to receiver production:

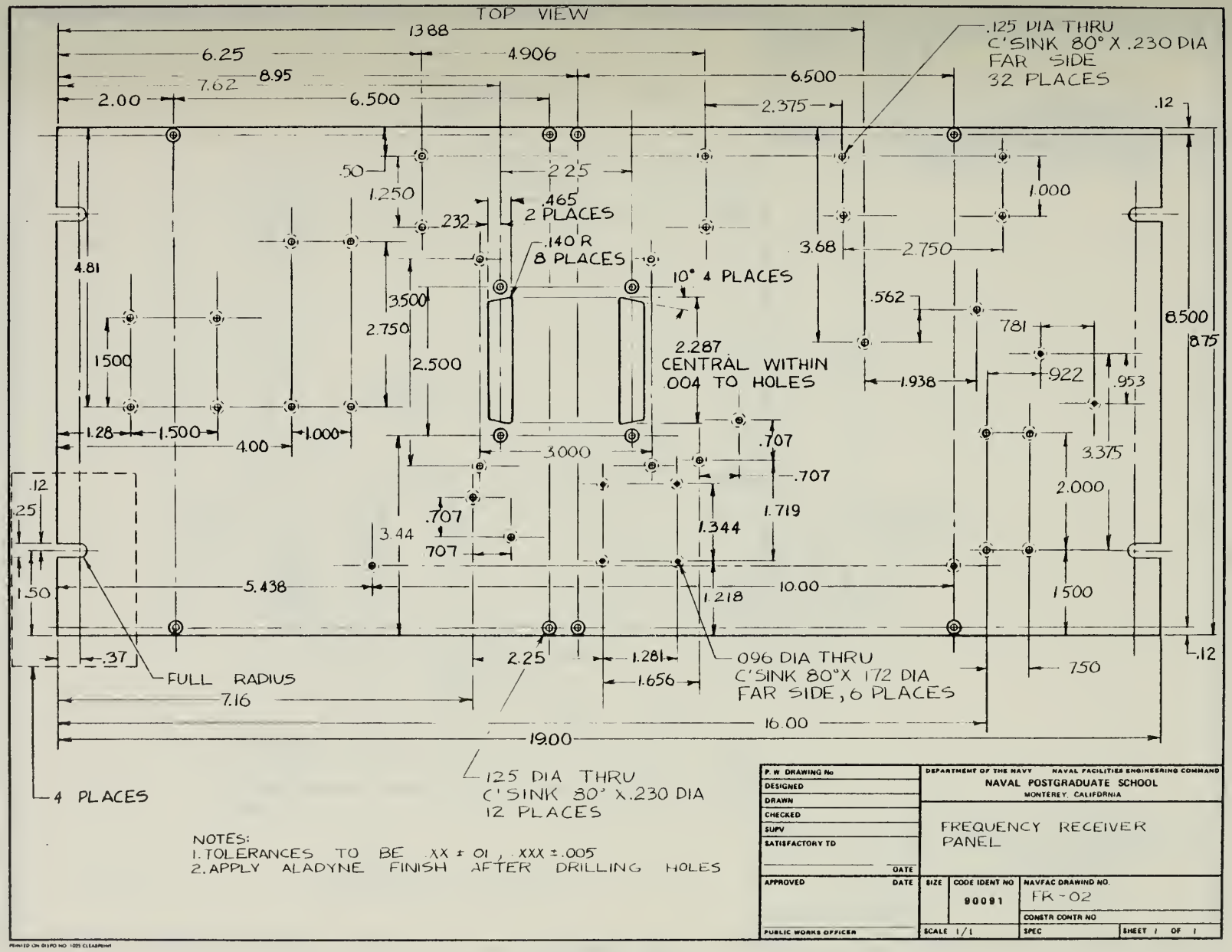
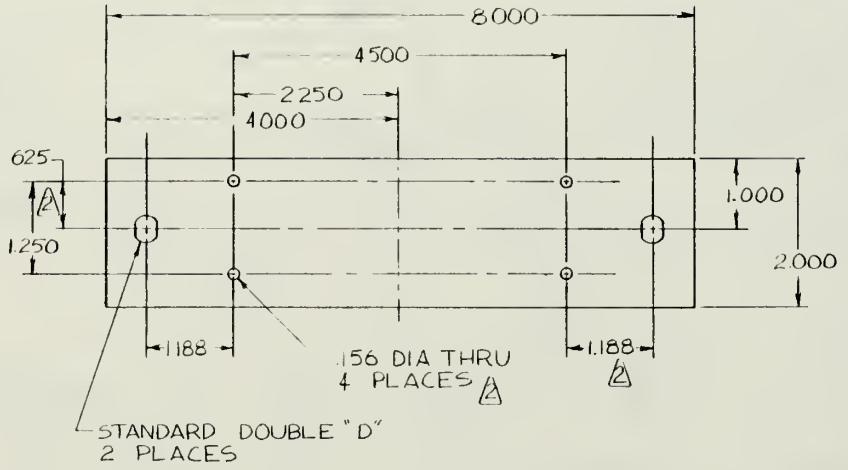


Figure 27
Panel Drill/Cutout Drawing



NOTES:
1. TOLERANCES TO BE .XX ± 01, XXX ± .005
2. MODIFICATION TO PART

REVISION LTR	DATE
	DATE
	DATE
	DATE
	DATE
DRAWN BY	DATE
APPROVED BY	DATE

DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

ANALOG CASE/PANEL

DRAWING NUMBER FR-11 | SHEET 2 OF 2

Figure 28
Analog Signal Processor RFI Box

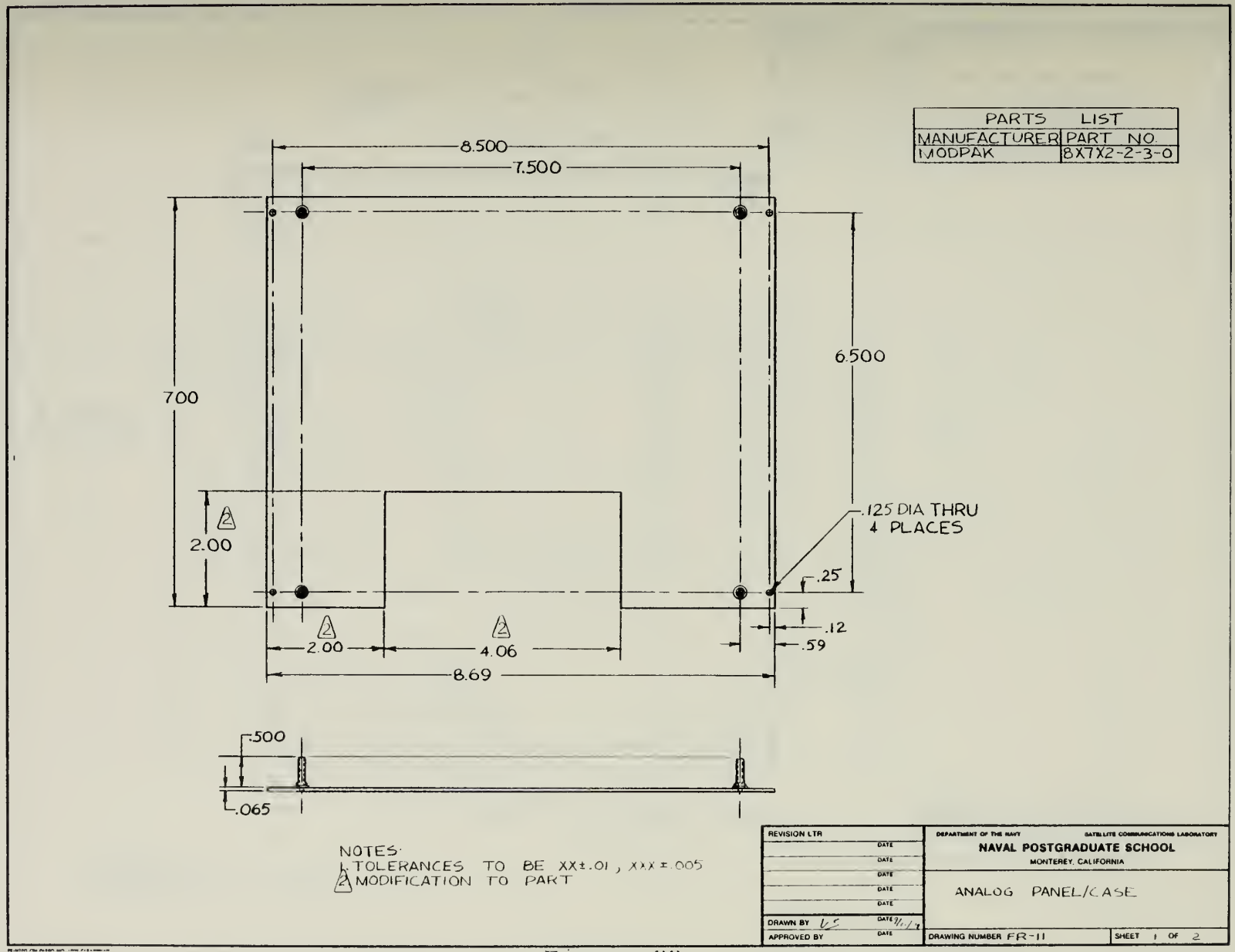


Figure 29
Analog Signal Processor RFI Box-Base Plate

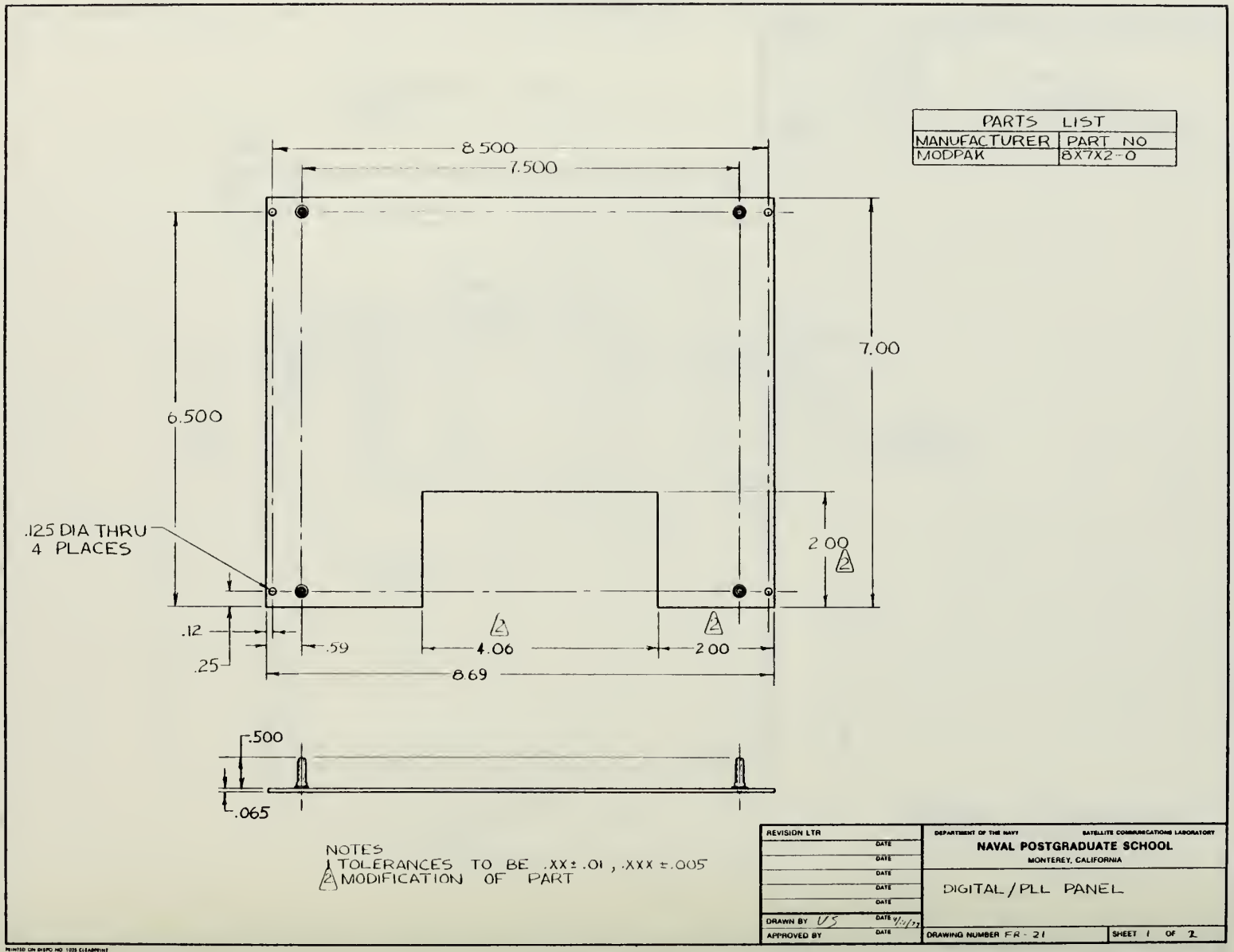


Figure 30
Digital/PLL Signal Processor RFI Box-Base Plate

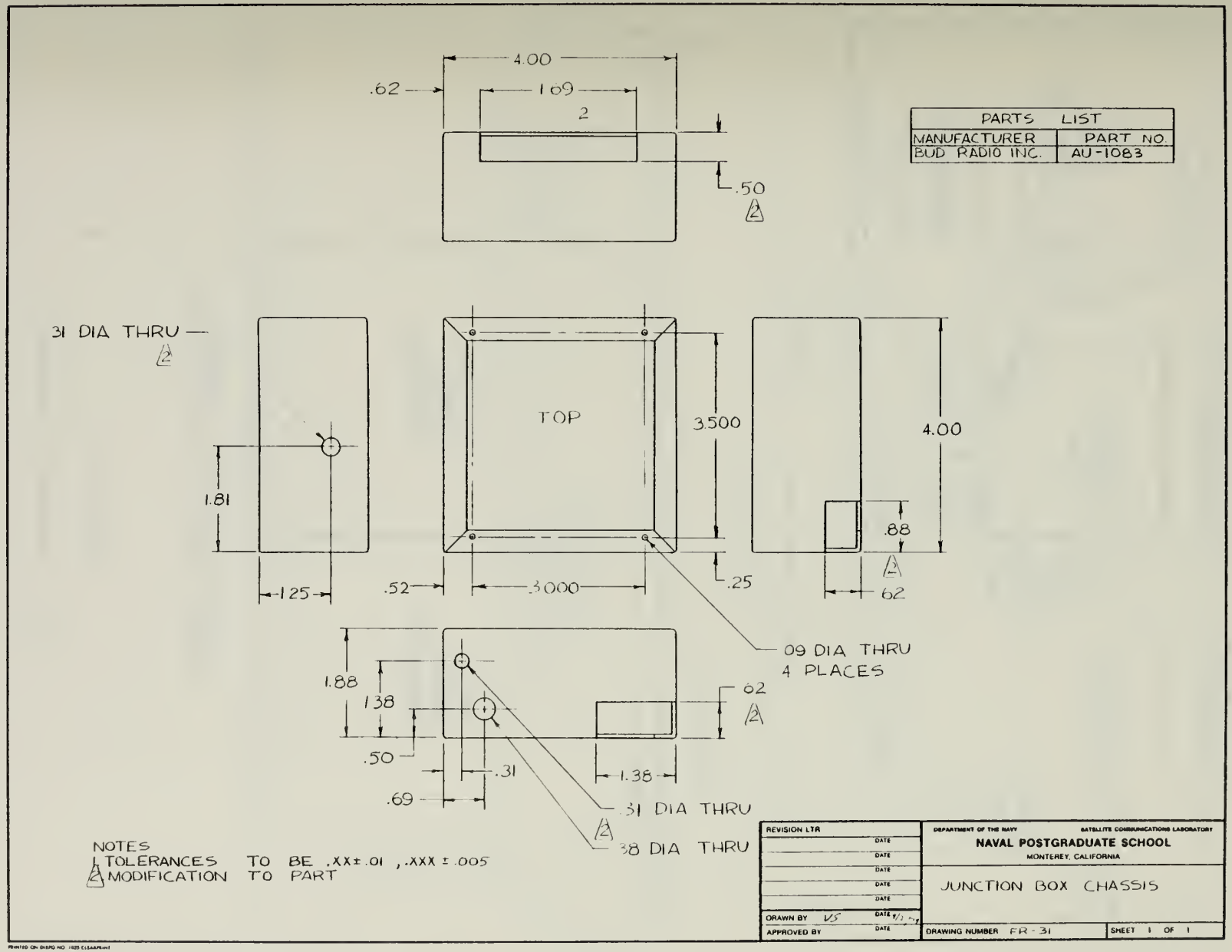
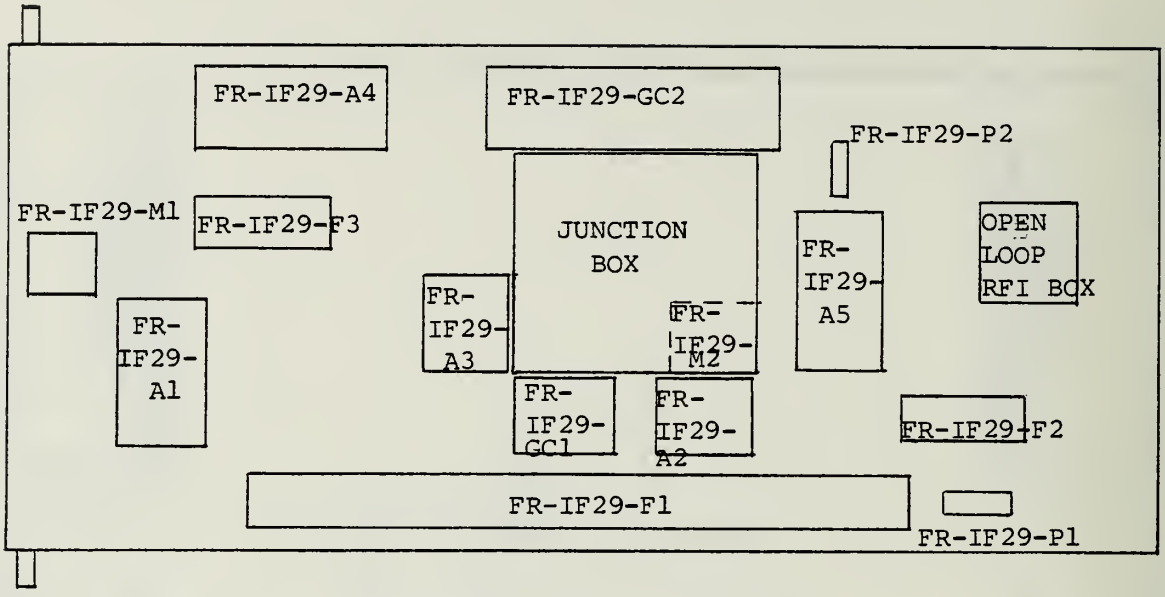
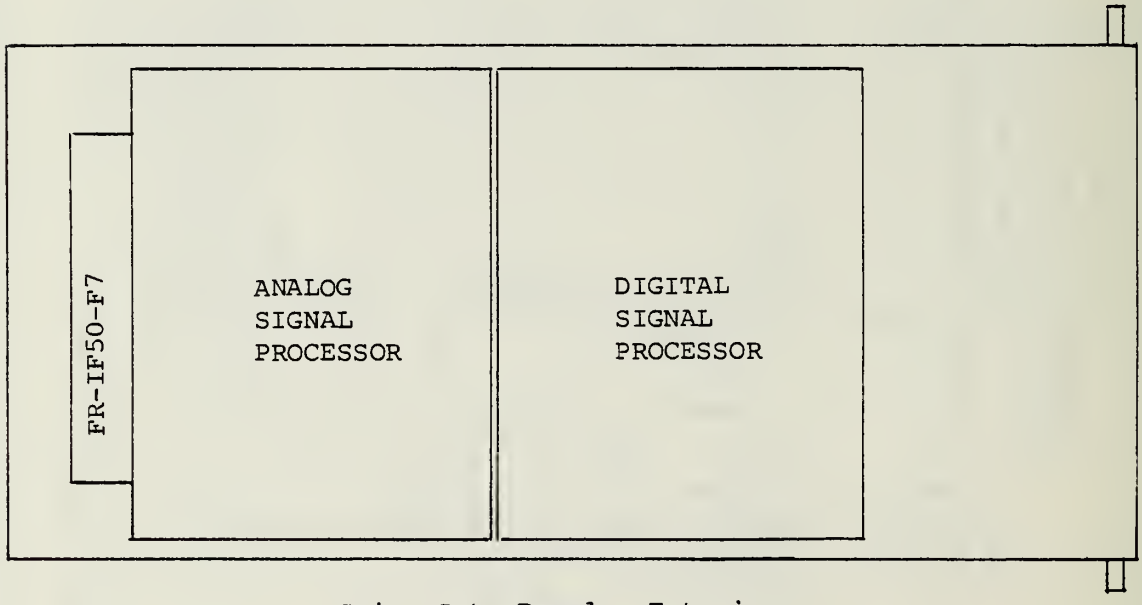


Figure 31
Junction Box Drawing



Swing Gate Panel - Interior



Swing Gate Panal - Exterior

Figure 32

Panel Assembly Drawings

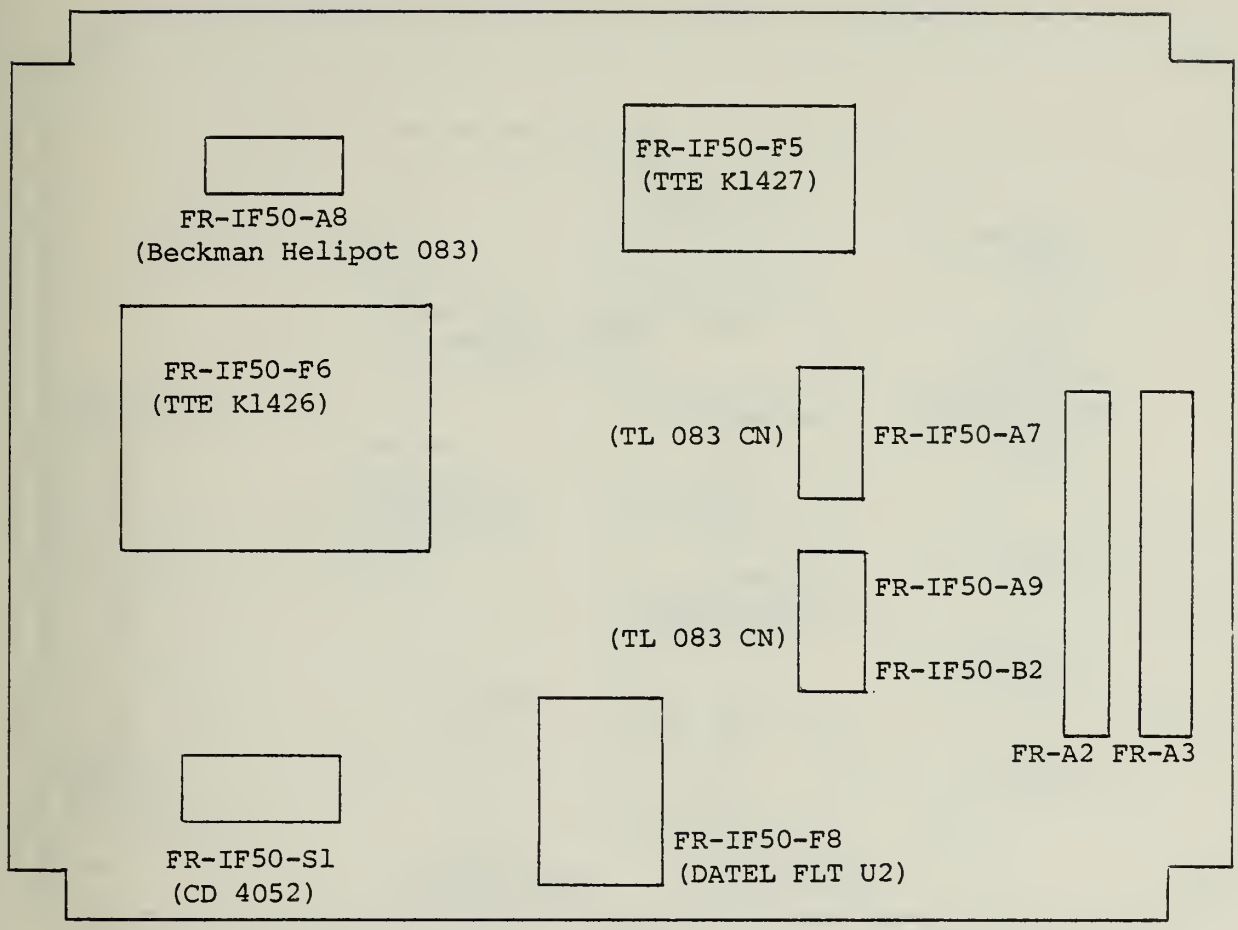


Figure 33

Filter Bank PC Board Layout

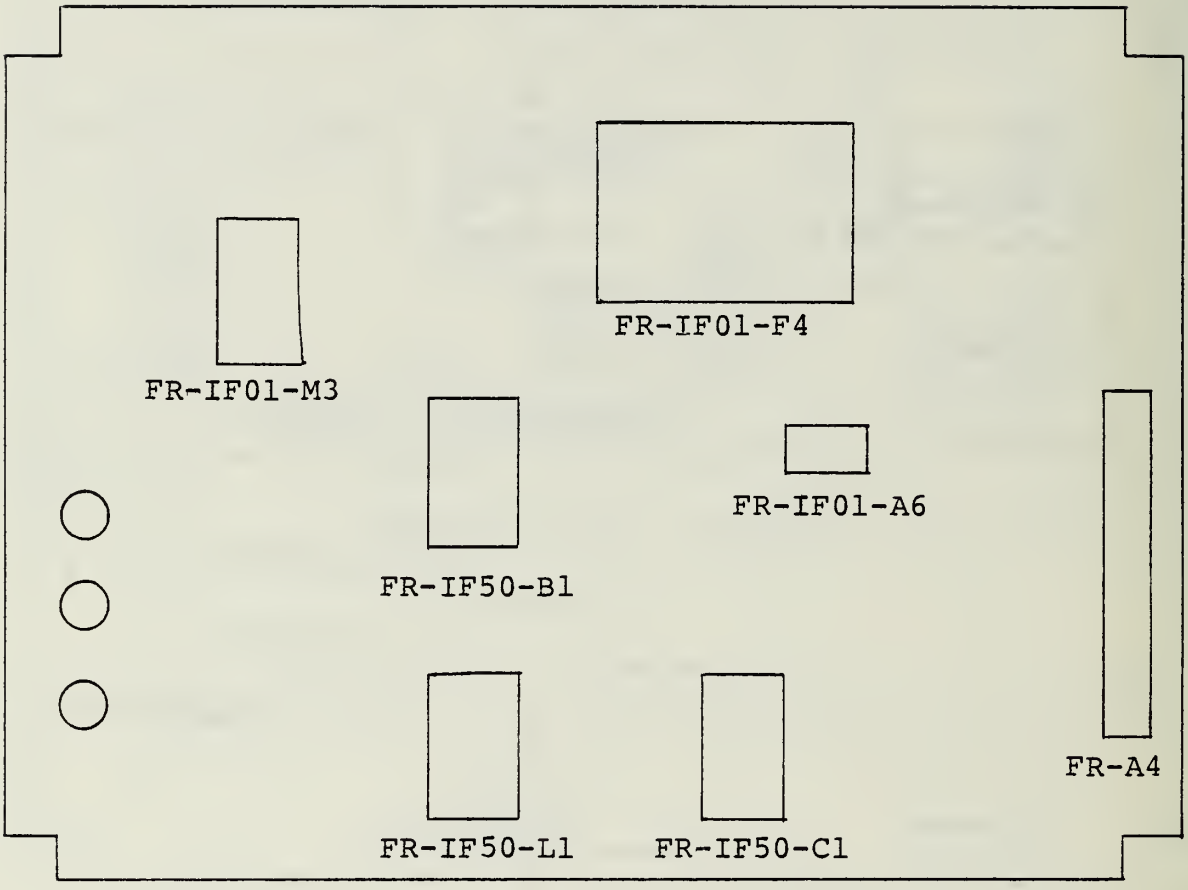


Figure 34

Analog Signal Processor PC Board Layout

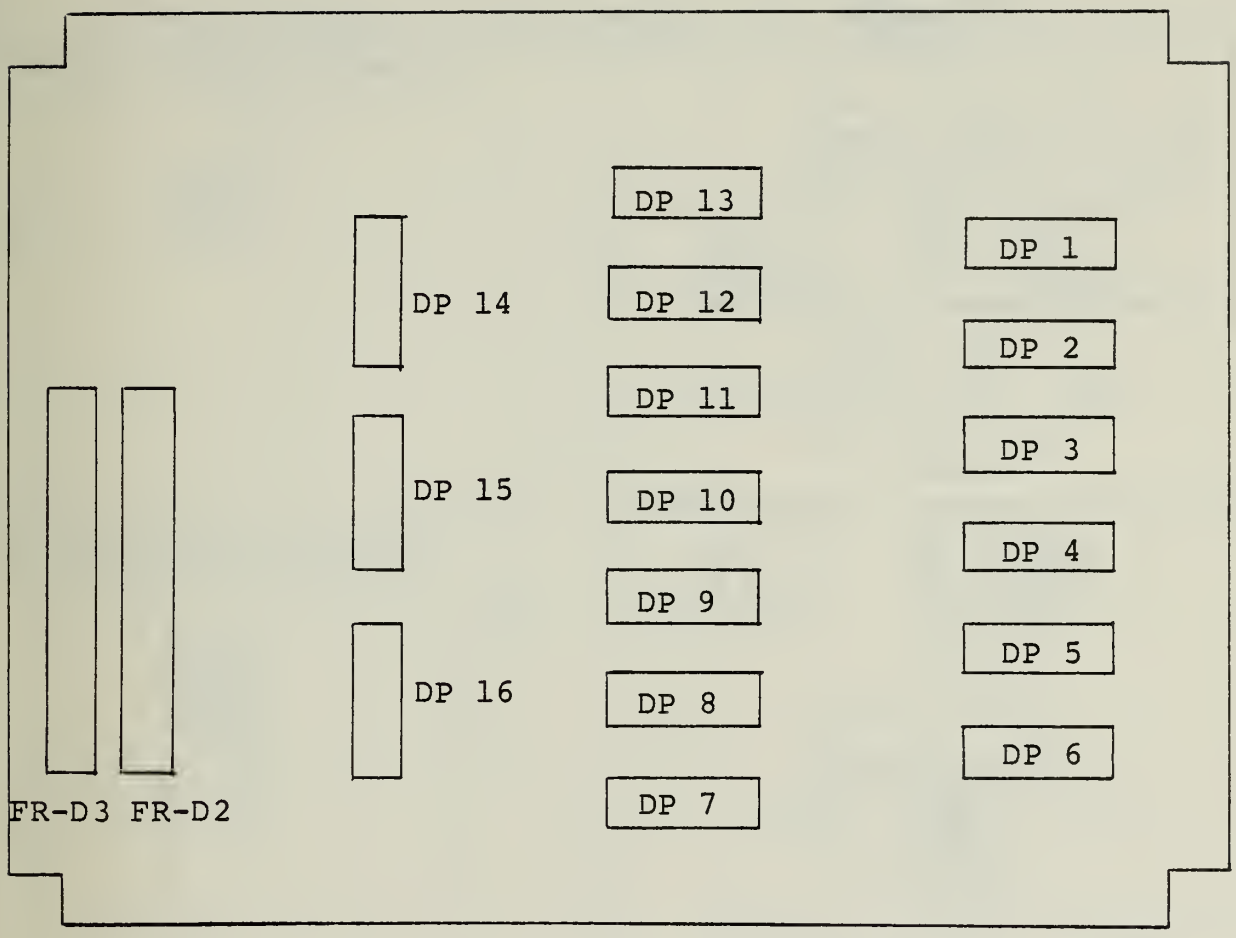


Figure 35

Digital Signal Processor PC Board Layout

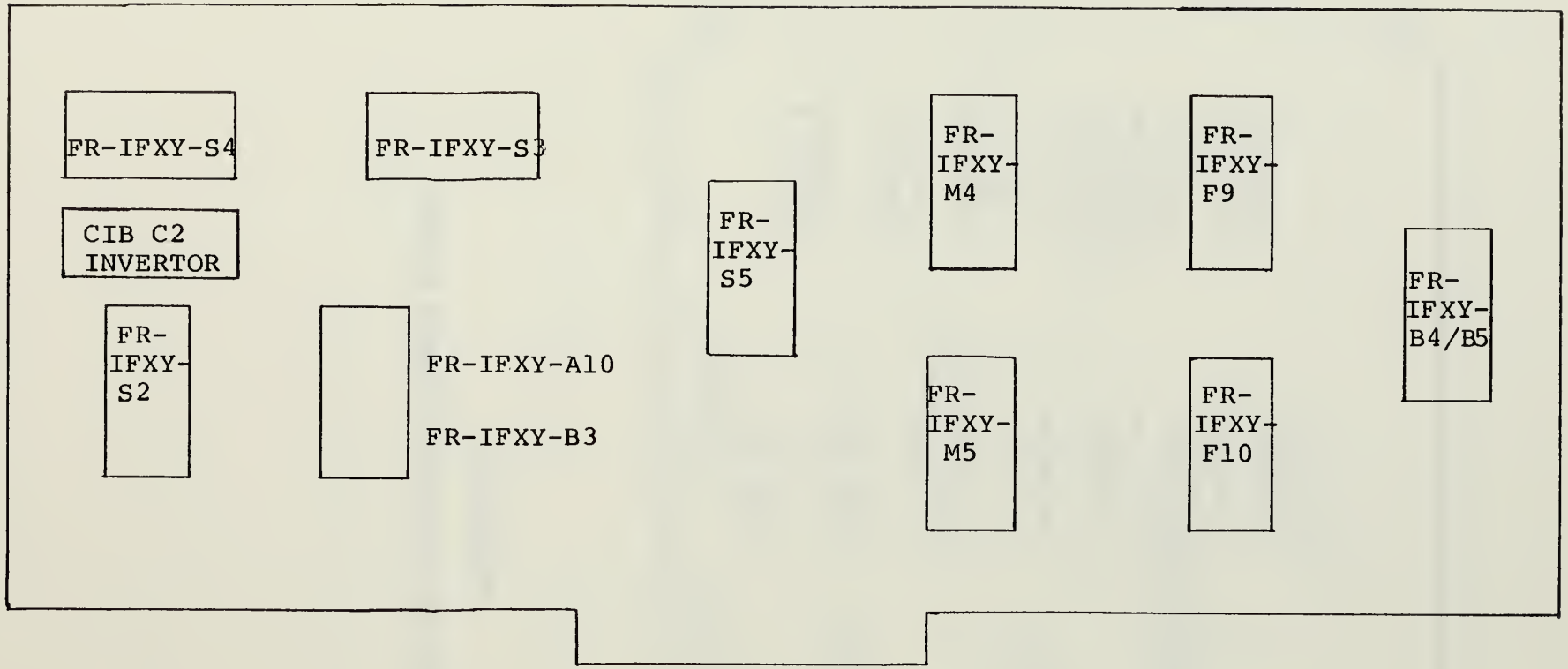


Figure 36

X-Y PC Board Layout

CONNECTOR NUMBER	PIN NUMBER	CONNECTION
Digital Signal Processor Board Connections	1	+5
	2	Loop Filter Gnd
	4	Lock Comparitor Gnd
FR-D1	6	Lock Comparitor Signal
FR-D2	8	Loop Filter Signal
FR-D3	10	CIB B3
	18	CIB B2
	20	Open Loop Sweep Frequency
	22	VCXO Output
	32	50 kHz $\angle 90 - \emptyset$ (out)
	34	50 kHz $\angle 0 - \emptyset$ (out)
	36	200 kHz (in)
	37	Ground
Analog Signal Processor Board Connections	1	Ground
	3	+15 VDC
	4	-15 VDC
FR-A1	5	-12 VDC
FR-A2	6	+12 VDC
FR-A3	8	Limiter Input (-)
FR-A4	10	X-Y Input (+)
	12	Limiter Input (+)
	14	Filter Bank In (+)
	16	Filter Bank In (-)
	18	CIB A2
	20	CIB A1
	33	VCXO/Manual Lock Frequency
	35	1 MHz IF In
	37	Ground

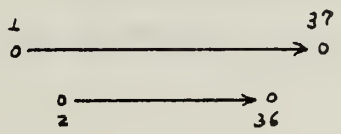


TABLE XIII

FREQUENCY RECEIVER PIN CONNECTIONS

CONNECTOR NUMBER	PIN NUMBER	CONNECTION
XY-1	1	-12 VDC
	2	Ground
	3	+12 VDC
	4	CIB C1
	5	FR-1 (+)
	6	FR-2 (+)
	7	CIB C2
	8	FR-1 (-)
	9	CIB C3
	10	FR-2 (-)
	11	CIB C4
	13	CIB C5
	14/15	+5 VDC
	16	50 kHz $\angle$ 0 - Ø from FR-1
	17	50 kHz $\angle$90 - Ø from FR-2
	18	50 kHz $\angle$ 0 - Ø from FR-2
	19	50 kHz $\angle$90 - Ø from FR-1
	20	X Input to X ADC
	21	Y Input to Y ADC
	22	X Output to scope
	23	Y Output to scope
	24	Ground

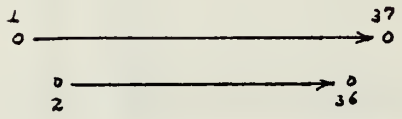


TABLE XIV

X-Y DISPLAY DRIVER PIN CONNECTIONS

ITEM	QUANTITY
Merrimac Mixer-DMM-4-250	2
ANZAC Amplifier - AM 102	2
ANZAC Amplifier - AM 105	1
ANZAC Amplifier - AM 108	2
K&L Tubular Filter - 4B340-29/1.-0	1
K&L Lamped Filter - 4B50-29/2.5-0	1
Tyco Crystam Filter - 001-34-760	1
Daico Step Attenuator - 100C1428-1D	1
Daico Step Attenuator - 100D0589-6 -A-.5,1,2,4,8,32	1
Narda 3dB Attenuator - SMA	2

TABLE XV

29 MHz IF Stage Parts List

	ITEM	QUANTITY
FILTERS	TTE Bandpass Filter K1426	1
	TTE Bandpass Filter K1427	1
	Comstrom Seg. Bandpass Filter	1
	DATEL FLT-U2 Active Filter	1
IC's	Analog Switch CD4052 BE	1
	Beckman Helipot 083 Driver	1
	TL083CN OPAMP	2
	+12 V DC Regulator (7812)	1
	-12 V DC Regulator (7912)	1
CONNECTORS	DC-37PV	1
	DC-37SV	1
RESISTORS	39Ω	1
	600Ω	2
	1kΩ (1%)	2
	3kΩ (1%)	1
	6.8kΩ	1
	10kΩ	2
	14kΩ	1
	15kΩ	1
	18kΩ (1)	1
	32kΩ	2
	33kΩ	1
	100kΩ	1
CAPACITORS	200pF	1
	0.1 μF	5
	2.2 μF	2
POTENTIO-METERS	Bourne RJ26FW103(1kΩ)	3

TABLE XVI

Filter Bank Parts List

	ITEM	QUANTITY
FILTERS	TTE Bandpass Filter K17C	1
IC's	Balanced Demodulator MC 1496	1
	LM 318 OPAMP	1
	TL 083 CN OPAMP	1
	SL 1624C	1
	NE 527A Voltage Comparator	1
DIODES	1N5221B	2
RESISTORS	50Ω	1
	100Ω	1
	820Ω	1
	1kΩ	5
	1.5kΩ	2
	3kΩ	3
	10kΩ	6
	1MΩ	
	5pF	1
	0.001 μF	2
	0.1 μF	10
	1.0 μF	1
POTENTIOMETERS	Bourne RJ26FW103(50kΩ)	1
CONNECTORS	DC-37PV	1

TABLE XVII

Analog Signal Processor Parts List

	ITEM	QUANTITY
IC's	7400	4
	7402	1
	7474	1
	7486	3
	74H108	2
	74121	3
	74153	1
	74177	1
RESISTORS	2k	2
	3.9k	1
	1k	1
	200	1
	120k	1
POTENTIOMETERS	Bourne RJ26FW201(200)	2
	Bourne RJ26FW105 (100k)	1
	10μ	2
	0.1μ	7
	1000p	3
SWITCHES	Alco MSP205R	1
CONNECTORS	DC-37PV	1
	DC-37SV	1

TABLE XVIII

Digital Signal Processor Parts List

	ITEM	QUANTITY
BOX	BUD AU-1083	1
CONNECTORS	Amphenol 904-112(SMA)	2
	TRW Cinch DC-37S	4
	Amphenol MS3102-A-145-7P	1

TABLE XIX

Junction Box Parts List

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